5-1/4'' Winchester Disk Drive Controller Service Manual

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MAI BasicFour®

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PREFACE

This manual provides service information for the Winchester Controller for the 5-1/4 Inch Disk Drives. This information is presented as an aid for field service personnel, and supports the installation, operation, and maintenance of the Controller.

The major topics covered in this manual are:

Section 1	Introduction
Section 2	Installation
Section 3	Functional Description
Section 4	Maintenance
Section 5	Removal/Replacement
Appendix A	Single-Board WDC Maintenance Aids
Appendix B	Two-Board WDC Maintenance Aids

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures that may be required to correct the interference.

The use of shielded I/O cables is required when connecting unit to any and all optional peripheral or host devices. Failure to do so may violate FCC rules.

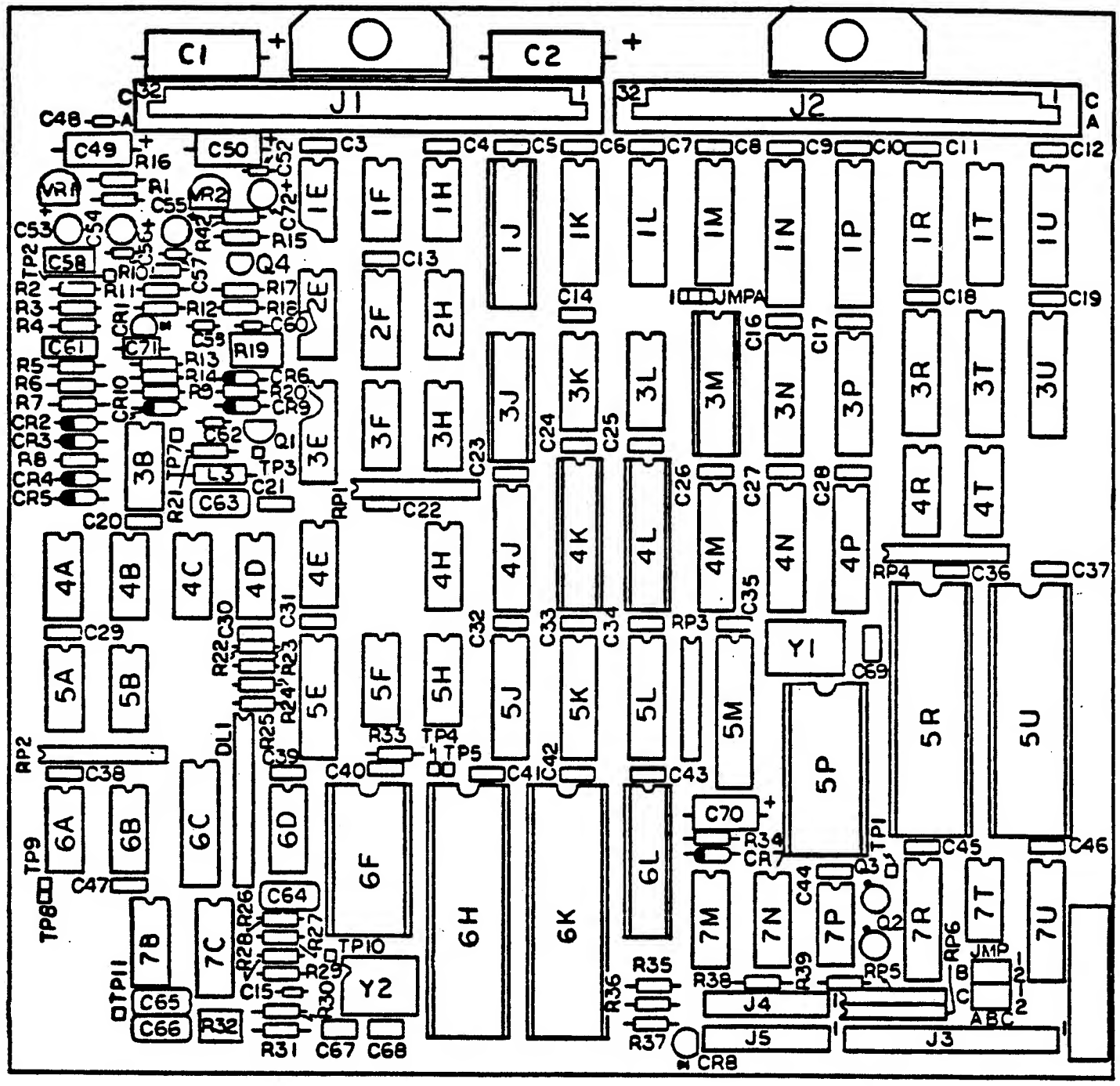


Figure 1-1. 5-1/4 Inch Winchester Disk Drive Controller

SECTION 1

INTRODUCTION

1.1 GENERAL

The Winchester Disk Drive Controller (WDC), Figure 1-1, provides the means by which an BOSS IX system communicates with one or two 5-1/4" Winchester disk drives. The controller is comprised of two functionally independent sections, an Adapter section and a Controller section. The adapter section provides an interface between the host's I/O bus and the SCSI (Small Computer System Interface) bus in the WDC.

In the current version of the WDC, Part No. 903496, the Adapter section and the Controller section are physically combined on a single PCBA (printed circuit board assembly). In the older version of the WDC, Part No. 903439, the SCSI Bus Adapter, Part No. 907649, is mounted "piggy-back" style on top of the controller portion. Either configuration allows the WDC to support one or two Winchester disk drives with disk capacities ranging from 10 to 190 megabytes.

Table 1-1 lists the 5-1/4" Winchester (fixed) disk drives that are supported by the WDC.

1.2 PCBA DESCRIPTION

1.2.1 Single-Board WDC

The single-board WDC consists of a PCBA which is designed for I/O stack mounting in the system housing. All components are mounted on one side of the board and soldered except for the microprocessor and sequencer, all PAL (program array logic) chips, PROM and static RAM chips, encoder/decoder chips and buffer controller chips. These ICs are socketed for ready exchange or replacement. In addition to the electronic and electrical components, the PCBA also contains three jumper blocks, a (green) LED indicator and five electrical connectors, whose locations are shown in Figure 1-2.

NOTE

The single board WDC is not supported in the MAI 3000 system.

Table 1-1. 5-1/4" Winchester Disk Drives Supports by the WDC

Vendor Model Number	MAI ID	Unform. Capac. MByte	Format. Capac. MByte	Number of Tracks	Number of Heads	Bytes per Sector	Sectors per Track	Number of Cylinders	Average Access Time	Used On System
1085	85	85.32	71.3	8192	8	512	17	1024	28 MSEC	2000 3000
1105	90	105.1	87.89	10098	11	512	17	918	27 MSEC	2000 3000
1140	123	143.4	126.9	13770	15	1024	9	918	27 MSEC	1500
1140	120	143.5	119.85	13770	15	512	17	918	27 MSEC	1500 2000 3000
2190	190	191.24	159.81	18360	15	512	17	1224	30 MSEC	3000
1304	43	51.9	43.35	4980	6	512	17	830	30 MSEC	1600 2000
1304	86	103.8	86.69	9960	12	512	17	830	30 MSEC	(1) 1600 (2) 2000
1324	43/60	64	43.35	6144	6	512	17	1024	28 MSEC	(3) 2000
1325	65/75	85.3	71.3	8192	8	512	17	1024	28 MSEC	2000
201	10	13.33	10.49	1280	2	256	32	640	90 MSEC	S10
202	20	26.66	20.97	2560	8	256	32	320	90 MSEC	S10
202	20	26.66	22.28	2560	8	512	17	320	90 MSEC	1600 2000
202	44	53.32	44.56	5120	16	512	17	320	90 MSEC	(4) 1600
203E	30	40	33.42	3840	6	512	17	640	55 MSEC	2000
203E	30	40	31.46	3840	6	512	17	640	55 MSEC	1500
204E	40	53.33	44.56	5120	8	512	17	640	55 MSEC	2000
ST225	20	25.62	20.15	2460	4	512	17	615	65 MSEC	1500
ST4026	20	25.62	20.15	2460	4	512	17	615	40 MSEC	1500

NOTES:
(1) DUAL 43'S
(2) DUAL 43'S
(3) NEW 43MB DRIVE
(4) DUAL 22'S

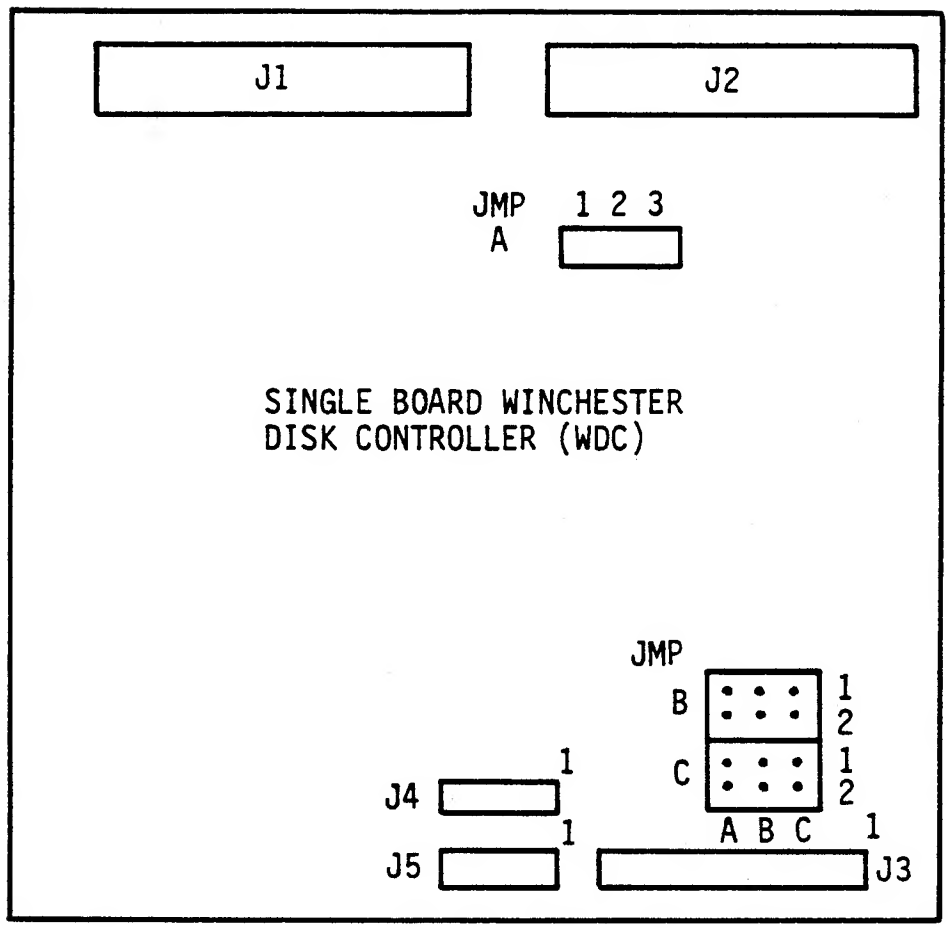


Figure 1-2. WDC PCBA Location of Major Components

1.2.2 Two-Board WDC

The two-board WDC consists of a PCBA containing the Controller section of the WDC which is mounted, piggy-back style, onto the PCBA containing the Adapter section. The WDC, consisting of both boards, is mounted on the I/O stack in the system housing. All components of the boards are mounted on one side of the board and soldered except for the microprocessor and sequencer PAL (program array logic) chips, PROM and static RAM chips, and selected encoder/decoder chips. These ICs are socketed for ready exchange or replacement. In addition to the electronic and electrical components, the Adapter also contains an 8-position DIP switch, a (green) LED indicator, and three electrical connectors. DC power is applied to the Adaptec Controller through a four-pin cable assembly which is hard-wired to the Adapter board. The Adapter board is similarly equipped except that no DC power connection is required. See Figure 1-2.

1.3 ADAPTER SECTION FEATURES

The Adapter section operates as a Type 1 bus master and will DMA 16 bits at a time; that is only on DMA word boundaries. Overall operations performed by the Adapter section include:

- Programmable vectored interrupt to the host when a disk command or disk seek is completed (single-board WDC only). The interrupt is hard-wired as a level 2 interrupt (7 is highest). Interrupts can be enabled or disabled by host command.

- DMA and interrupt arbitration with up to 15 other controllers for control of the BOSS IX system I/O bus when requesting a DMA transfer or during an interrupt acknowledge cycle.

- Provisions for allowing one or two WDCs (single-board WDC only) to operate independently on an BOSS IX system I/O bus, using jumper blocks on the PCBA.

- Bi-directional data/driver registers or transceivers which combine two 8-bit data latches for input and two 8-bit data latches for output to form two 16-bit registers.

- Address registers and drivers consisting of six 4-bit register/counter/driver devices capable of addressing the BOSS IX system main memory as follows:

  32 megabytes on the single-board WDC
  2 megabytes on the two-board WDC

- Control logic which provides the appropriate interface between the BOSS IX system I/O bus and the controller's SCSI bus. The logic starts DMA or Interrupt cycles when necessary and handles packing and unpacking of the data transferred between the 16-bit I/O bus and the internal 8-bit bus.

1.4 CONTROLLER SECTION FEATURES

The Controller section consists of a daisy-chained control bus and a radial data bus.

The control bus handles all the control functions of the disk drive/controller interface, primarily in the form of ±5-volt DC control signals. The radial data bus handles read and write MFM data in the form of differential signals. Write precompensation can be set for either Drive 0 or Drive 1 by means of jumpers on the PCBA. (In a two-board controller, write precompensation is NOT individually selectable for each drive.) Also, precompensation may be set to be always on, always off, or enabled at and beyond the reduced write current cylinder, using the jumpers.

Overall operations performed by the Controller section include:

- Support for standard SCSI commands, including a high speed data search command.

- A dual-ported 1k-byte data buffer for rapid data transfers with no sector interleaving required.

- Transparent (to the host) disk defect handling. No spare tracks are required, eliminating long seeks to alternate tracks.

- Programmable logical addressing to access variable length (256, 512 or 1024 byte) blocks.

- Self configuring on power up, including: reading and storing drive parameter data on Track 0; and copying and saving the largest block address and defect counts.

- Multiple block data transfers and implied Seek, by imbedding logical block addresses within the basic Read and Write requests.

- Host-programmable disk parameters such as number of cylinders, heads and sectors. Sector interleaving and sector size, as well as step type and rate, are also programmable by the host.

- (On the single-board WDC) Interrupt-driven overlapped Seek operations, which allows one drive to be available for use while the other is seeking. The Seek Complete interrupt can be enabled and disabled by host command.

1.5 SPECIFICATIONS

Table 1-2 provides the specifications for the WDC.

Table 1-2. Winchester Disk Drive Controller Specifications

PHYSICAL

Width:
- Single Board: 8.8
- Two-Board Adapter: 8.8
- Two-Board Controller: 8.8

Depth:
- Single Board: 8.6
- Two-Board Adapter: 8.6
- Two-Board Controller: 8.6

ENVIRONMENTAL

Operating Temperature:
32°F to 122°F (0°C to 50°C)

Operating Humidity
20% to 80% (non-condensing)

ELECTRICAL

Power: +5VDC ±5%
-12VDC +5%

1.6 RELATED PUBLICATIONS

The following servicing documentation may be used in conjunction with this publication for the 5-1/4" Winchester Disk Controller:

- M8079, MAI 2000 System Service Manual
- M8083, 5-1/4" Fixed Media Disk Drive Service Manual
- M8108, MAI 3000 System Service Manual

SECTION 2

INSTALLATION

2.1 GENERAL

This section contains unpacking/packing instructions and installation requirements for the single-board and two-board WDC.

2.2 SINGLE BOARD WDC

2.2.1 Unpacking/Packing Instructions

The single-board WDC is shipped in an anti-static bag, inserted between two layers of styrofoam and sealed in a cardboard shipping carton. Unpack the WDC as follows:

1. Prior to accepting the package from the carrier, inspect the shipping carton for signs of external damage. Any indication of external damage must be noted on the carrier's shipping form and reported immediately to the MBF Sales Office.

NOTE

When unpacking the PCBA, set aside the packing materials and shipping carton for use if it should become necessary to reship. The PCBA is ESD sensitive. Proper handling procedures should be used.

2. With the PCBA shipping carton in its upright position, open the carton and carefully remove the PCBA.

3. Unwrap the PCBA and inspect it for signs of shipping damage. Immediately report any damage to the MBF Sales Office.

2.2.2 Installation Requirements

Install the single-board WDC as follows:

WARNING

Dangerous voltages exist within the Base Unit of the BOSS IX system. Be sure that the power is turned off and the power cord is removed before opening the Base Unit cover.

1. Shut down the system, turn the Base Unit off and remove the power cord.

2. To prepare the MAI 2000 system, insert a screwdriver or similar device into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the plastic latch. Repeat for the left-hand latch and remove the cover.

3. To prepare the MAI 3000 system, perform the following:

   a. Remove the CCA front panel by using a screwdriver to disengage two captive screws at the bottom and then pulling from the bottom. If device controller boards, memory boards or drives are to be installed, remove the side panels also.

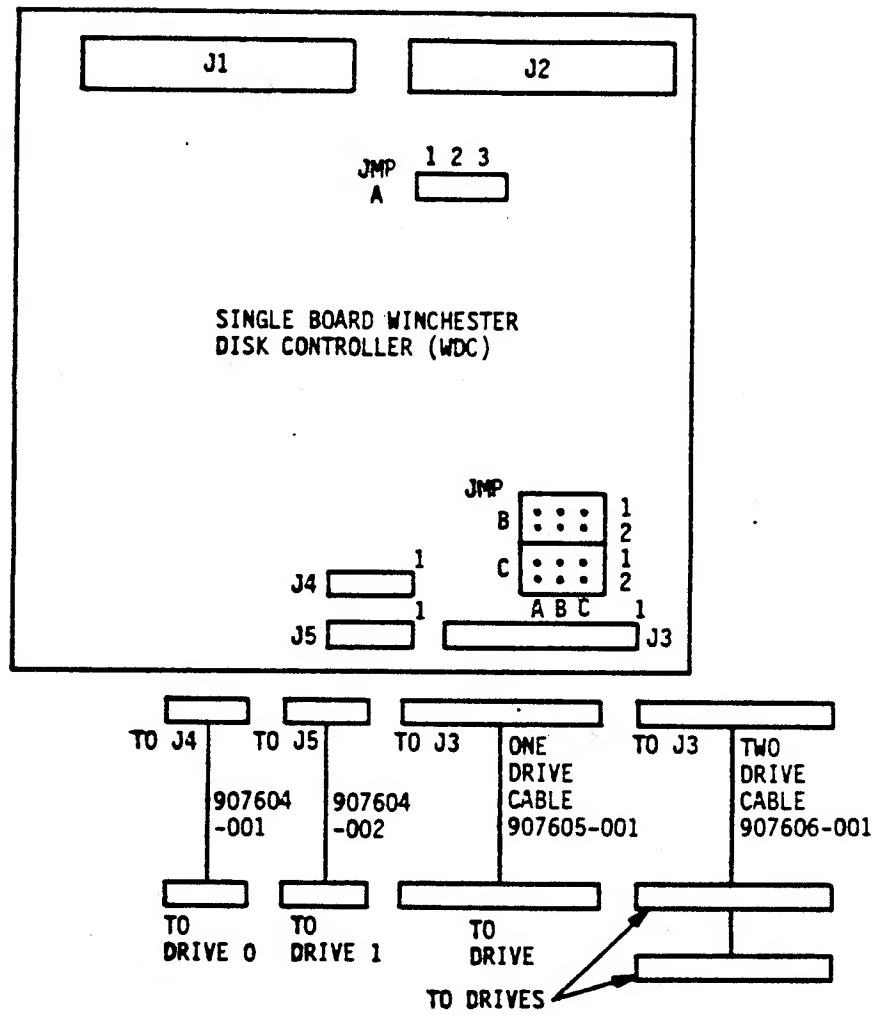
   b. The side panels slide forward for easy removal. It may be helpful to insert the tip of a flat-blade screwdriver between the front flange of the panel and the frame, about midway down the panel; carefully twist the blade to disengage the panel from the frame.

4. Remove the drive cables connected to board connectors J3, J4 and J5 (see Figure 2-1 for connector locations).

5. Prepare the replacement WDC board for installation by installing the appropriate jumpers and setting the dip switches as indicated in Figure 2-1.

6. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.

7. Reconnect the power cord. Follow the instructions in the appropriate BOSS IX System User Guide for operating the host system.



JUMP A, WDC BOARD ADDRESS

WDC	PCBA	JMP A	BOARD ADDRESS	PAL @ LOCATION 1J
0	903496-001	1-2	CCXXXX Hex	911017-001
1	903496-002	2-3	CDXXXX Hex	911017-007

NOTES: If one WDC is on the system bus, it must be PCBA 903496-001. If two WDC's are on the system bus, one must be PCBA 903496-001 and the other must be PCBA 903496-002. Combinations other than those shown are not allowed.

JUMP B & C, WDC WRITE PRECOMPENSATION

JMP B & C (1)	DRIVE TYPE
1A-2A	Maxtor: Micropolis 1300B, 1320 (Note 2)
1B-2B	Rodine (Note 3)
1C-2C	Micropolis 1300A (Note 4)

NOTES: 1. JMP B controls: drive 0 on the -001 assembly
drive 2 on the -002 assembly
JMP C controls: drive 1 on the -001 assembly
drive 3 on the -002 assembly
2. Write precompensation always off.
3. Write precompensation always on.
4. Write precompensation on at and above the reduced write current cylinder.

Figure 2-1. Single-Board Cable, Jumper and Switch Connections

2.3 TWO-BOARD WDC

2.3.1 Unpacking/Packing Instructions

Each board of the two-board WDC is shipped in an anti-static bag, inserted between two layers of styrofoam and sealed in a cardboard shipping carton. Unpack the WDC as follows:

1. Prior to accepting the package from the carrier, inspect the shipping carton for signs of external damage. Any indication of external damage must be noted on the carrier's shipping form and reported immediately to the MBF Sales Office.

NOTE

When unpacking each PCBA, set aside the packing materials and shipping carton for use if it should become necessary to reship. The PCBA is ESD sensitive. Proper handling procedures should be used.

2. With the PCBA shipping carton in its upright position, open the carton and carefully remove the PCBA.

3. Unwrap the PCBA and inspect it for signs of shipping damage. Immediately report any damage to the MBF Sales Office.

2.3.2 Installation Requirements

Install the two-board WDC as follows:

WARNING

Dangerous voltages exist within the Base Unit of the BOSS IX system. Be sure that the power is turned off and the power cord is removed before opening the Base Unit cover.

1. Shut down the system, turn the Base Unit off and remove the power cord.

2. To prepare the MAI 2000 system, insert a screwdriver or similar device into the slot at the bottom right-hand side of the Base Unit cover, and push in to disengage the plastic latch. Repeat for the left-hand latch and remove the cover.

3. To prepare the MAI 3000 system, perform the following:

   a. Remove the CCA front panel by using a screwdriver to disengage two captive screws at the bottom and then pulling from the bottom. If device controller boards, memory boards or drives are to be installed, remove the side panels also.

   b. The side panels slide forward for easy removal. It may be helpful to insert the tip of a flat-blade screwdriver between the front flange of the panel and the frame, about midway down the panel; carefully twist the blade to disengage the panel from the frame.

4. Remove the drive cables connected to connectors J0, J1 and J2 on the WDC Adapter PCBA (see Figure 2-2 for connector locations).

5. Prepare the replacement WDC for installation by installing the appropriate jumpers and setting the dip switches for the WDC Adapter PCBA and Controller PCBA as indicated in Figure 2-2.

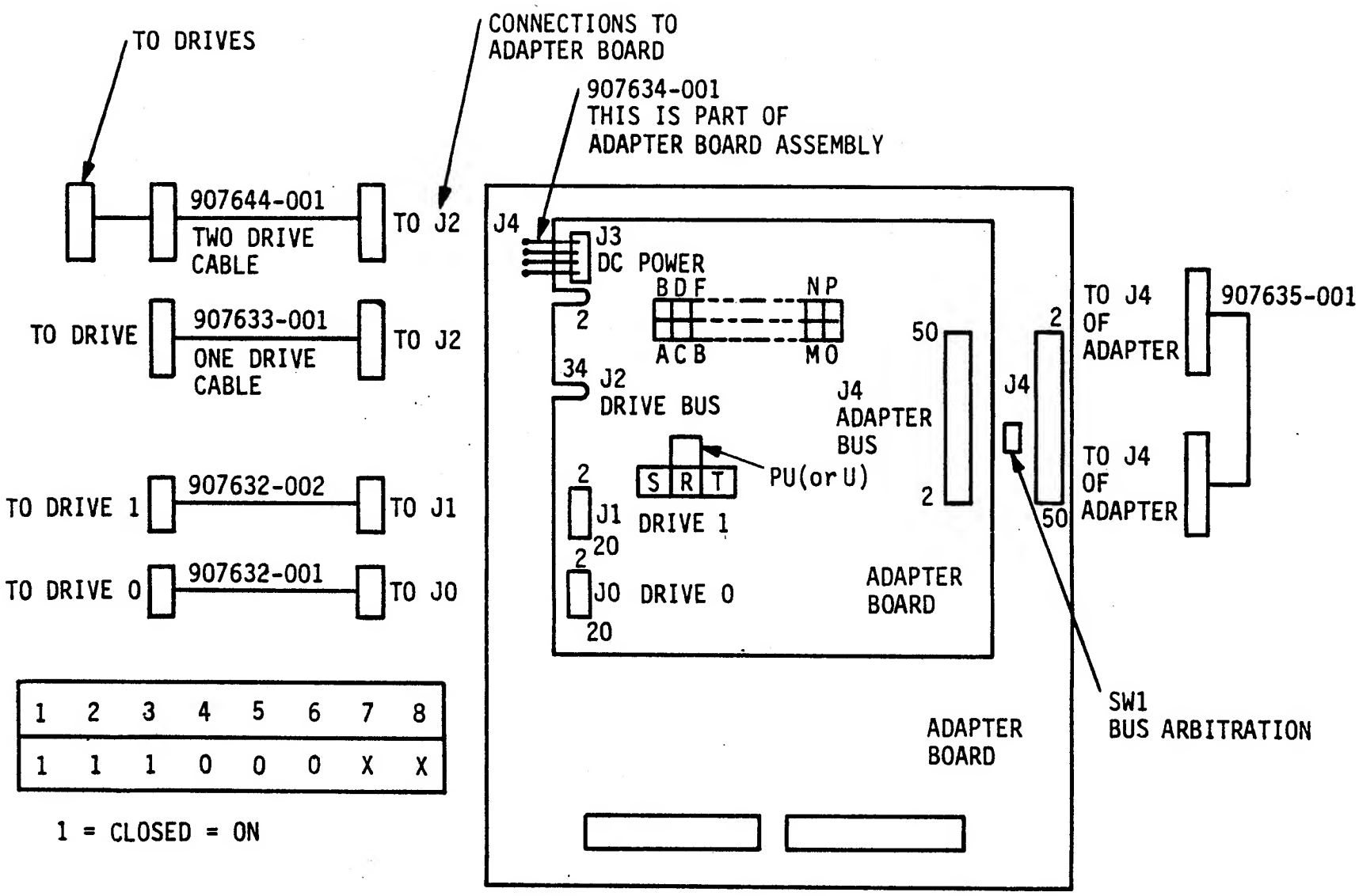
6. Locate the Adapter PCBA on the Controller PCBA in the position shown in Figure 2-2. The four plastic standoffs (one in each corner of the Adapter PCBA) should line up with the holes in the Controller PCBA. Press down on the corners of the Adapter PCBA until the retainers on the standoffs engage the Controller PCBA.

7. Install the power connector into connector J3 of the Adapter PCBA.

8. Install Adapter Drive and Bus cable and the CMB and Drive Bus cables as specified in Figure 2-2.

9. Replace the Base Unit cover by lowering the cover onto the Base Unit and allowing it to "snap" into place.

10. Reconnect the power cord. Follow the instructions in the BOSS IX System User Guide for operating the host system.



JUMPER CONNECTIONS

CONNECT FROM	TO	DRIVE 0	DRIVE 1	PROG. REDUCE WRITE CURRENT @ CYLINDER DRIVE 0	DRIVE 1
R	T	RODIME	NONE	132	-
R	T	RODIME	RODIME	132	132
R	S	RODIME	MICROPOLIS (1300A)	132	400
R	U	RODIME	MAXTOR/MICROP (1300B, 1320)	132	919/400
R	S	MICROPOLIS (1300A)	NONE	400	-
R	S	MICROPOLIS (1300A)	MICROPOLIS (1300A)	400	400
R	U	MICROPOLIS (1300A)	MAXTOR	400	919
R	U	MAXTOR/MICROP (1300B, 1320)	NONE	919/400	-
R	U	MAXTOR/MICROP (1300B, 1320)	MAXTOR/MICROP (1300B, 1320)	919/400	919/400

NOTES:

1. Drives 0 and 1 are for reference only. That is, if positions are switched, so are the parameters in the appropriate columns.
2. Jump position R-U is equivalent to no jumper installed.
3. Micropolis drive models 1304A & B and 1320 are used.
4. Rodime drive models 204, 203E and 240E are used.
5. Maxtor drive models XT1140 and XT1105 are used.

Figure 2-2. Two-Board Cable, Jumper and Switch Connections

SECTION 3

FUNCTIONAL DESCRIPTION

3.1 GENERAL

This section contains a functional description of the 5-1/4" Winchester Disk Controller (WDC) on three levels: a general block diagram description, a discussion of the system interface characteristics, and a detailed functional description of the WDC circuits.

Figure 3-1 is a functional block diagram of the WDC, showing the relationship of the Adapter section and the Controller section to the circuit elements with which they are involved. As indicated, the basic internal interface is the SCSI (Small Computer System Interface) bus. The 8-bit parallel SCSI bus handles all communication between the Adapter and the Controller sections.

NOTE

The MAI 3000 system does not support the two-board WDC.

3.1.1 Adapter Section Functions

The Adapter section provides an intelligent interface between the BOSS IX system I/O bus and the SCSI bus internal to the WDC. Primary bus control and interrupt priority are determined by the DMA and Interrupt Arbitration logic, which performs parallel arbitration with up to 16 other device controllers that may be connected to the I/O bus. Through this logic and the Control Logic circuit, the WDC responds to a Level 2 interrupt (with 0 being the highest), with a priority level which is lower than that of Memory Refresh, LAN controller or 4-Way controller in the system. PAL (Program Array Logic) devices are used in the Arbitration and Control circuits as well as in other circuits such as sequencing, interrupt acknowledge, addressing, status and overall control circuits, to establish logical patterns.

The Address and Bus Control unit determines if the WDC is being addressed by the host and which port is being used for communication. When the interrupt is acknowledged, an 8-bit value is placed on the BOSS IX system data bus which is used to create an interrupt vector. The vector is programmed into latches in the Data Transceiver and Latch circuit before a DMA is initiated. During the DMA cycle, a latch counter drives the BOSS IX system bus address lines and automatically increments the address (on an even word boundary) at the end of the cycle.

The Control, Vector and Status Registers are used for a variety of purposes by the host, which include: switching DMA on or off; enabling interrupts on the SCSI bus (disk drive Seek Complete, Command Complete); resetting the WDC; turning the LED control line on or off; polling the Status Register for WDC status information and making decisions based on the results.

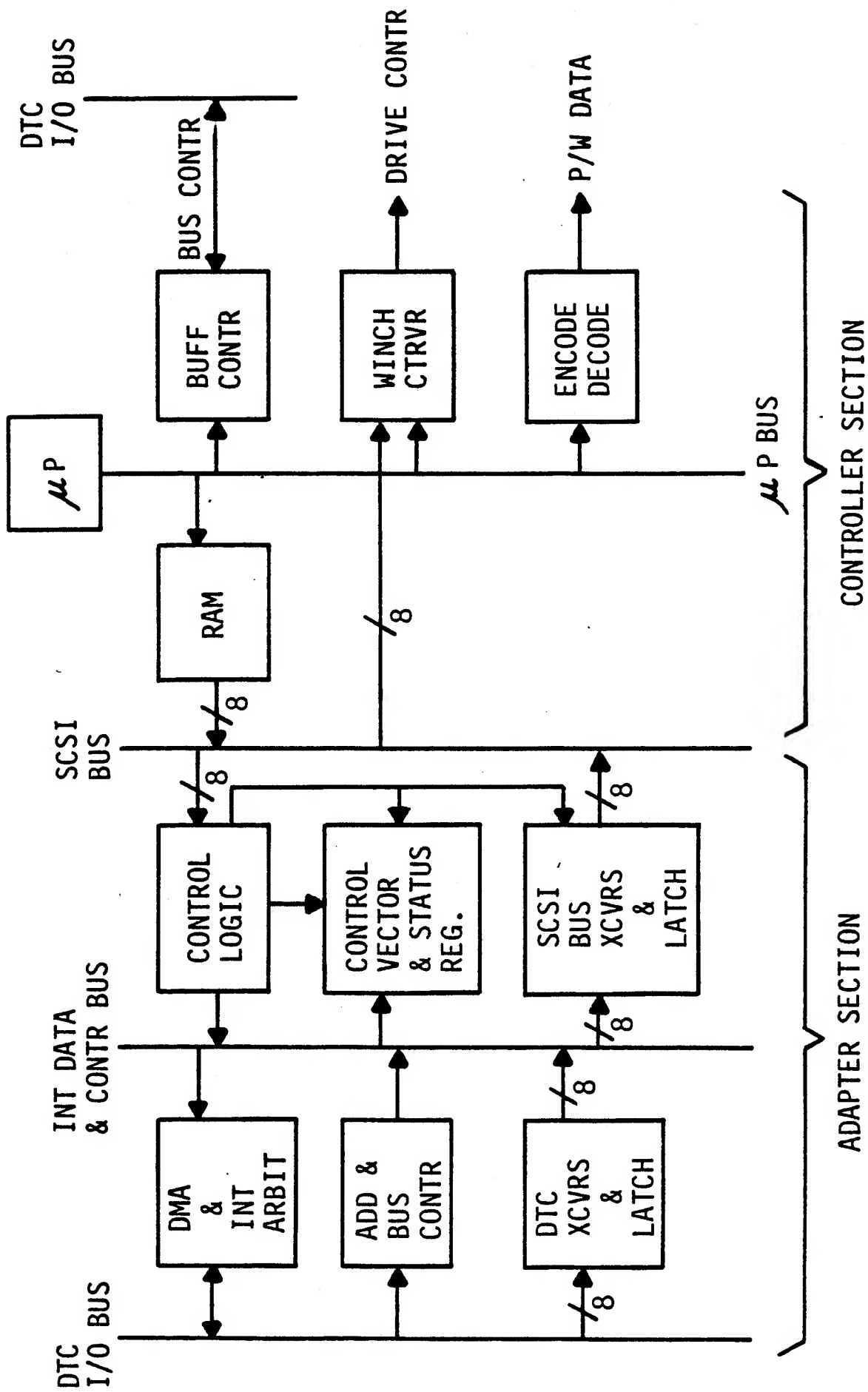


Figure 3-1. WDC Functional Block Diagram

The Data and SCSI Bus Transceivers are 8-bit bidirectional registers consisting of upper-byte and lower-byte segments. Associated with each segment is a pair of buffers (latches), one for input data and one for output data. The Data Transceivers handle all the BOSS IX system program I/O to and from the WDC, at odd-byte addresses. The Bus Transceivers handle all program I/O to and from the SCSI bus. The input buffers are also used during DMA Read from Memory to allow overlapped operations; the output latches buffer data during DMA Write operations to memory.

3.1.2 Controller Section Functions

The Controller section provides an intelligent interface between the internal SCSI bus and the ST-506 disk drive interface. The primary control unit in the Controller section is the 8085 Microprocessor. The Microprocessor communicates with the other logical elements in the Controller section over its own (Microprocessor) data bus. The RAM element is a 1K FIFO (first in first out) RAM buffer which transfers DMA data and control signals between the Microprocessor bus and the SCSI bus. The RAM is protected from overflow or underflow of data by the Buffer Control circuit. Through the RAM, the Buffer Control recognizes arbitration logic on the SCSI bus and controls direct memory access of data out of the FIFO RAM.

Buffer Control also controls the flow of synchronous data to/from the hard disk and the asynchronous SCSI interface, through the dual-port Winchester Controller circuit. The Encoder/Decoder includes the data separator functions needed to convert the MFM read data from the disk into a synchronized clock and NRZ data stream required by the SCSI bus. The Encoder/Decoder also performs the reverse conversion process; and it incorporates address mark generation and detection logic, as well as the write precompensation functions required for appropriate disk drive interface.

3.2 SYSTEM I/O INTERFACE

3.2.1 WDC I/O Addresses

The BOSS IX system assigns address block space in its memory by means of a combination of jumpers and board addresses. The jumpers allow the system to determine whether one or two WDCs are to operate independently on the system I/O bus. The board address defines the exact function the WDC is to perform. The jumper/board address assignments for single-board WDCs are specified in Figure 2-1. The jumper/board address assignments for the two-board WDC are as follows:

No. WDCs	JMP-A	Board Address
1	1-2	CCXXXX H
2	2-3	CDXXXX H

The address is loaded into the WDC address registers one byte at a time. Each byte must be acknowledged before the next byte can be loaded. The significance of each address is as follows:

- **Address CC0001** - Load DMA Address Register, HI byte
  Address CC0002 - Load DMA Address Register, MID byte
  Address CC0003 - Load DMA Address Register, LO byte

  These registers are loaded one byte at a time, with the 1's complement of the BOSS IX system address, right-shifted once.

- **Address CC0004** - Read Interrupt Vector Register

  The BOSS IX system initializes this register before using interrupt. The operation is required only once per DMA; it is not cleared with Reset.

- **Address CC0005** - Read/Write Control Register

  The Control Register contains control bits 0-5 and status bits 6-7. During a Write operation, only bits 0-5 are significant; during a Read operation, all eight bits are significant. Individual bits may be turned on or off using a single BSET or BCLR 68000 instruction. The register is cleared with Power On Reset. The significance of the bits is as follows:

Bit	Name	Read/Write	Function
Bit 0	SRST+	R/W	Reset the WDC. Bit must be maintained for a minimum of 25 microseconds; logically OR'd with POR and PFD.
Bit 1	LED-	R/W	LED control signal
Bit 2	INTEN+	R/W	ENA Oper Compl & Bus Error Interrupts
Bit 3	SEQEN+	R/W	Enable DMA
Bit 4	INTEND0+	R/W	ENA Drive 0 Seek Compl Interrupts
Bit 5	INTEND1+	R/W	ENA Drive 1 Seek Compl Interrupts Bits 4 and 5 used for buffered seek type drives only; set before issuing Seek command; reset before leaving interrupt service routine.
Bit 6	INTD0+	R Only	Drive 0 Seek Compl Interrupt Status
Bit 7	INTD1+	R Only	Drive 1 Seek Compl Interrupt Status

- **Address CC0008** - Host Write to Output Register

  This address byte is written to by the host during I/O data transfer (Information Transfer Phase) Host to Controller) operations.

- **Address CC0009** - Read Adapter's Status Register

Bit	Name	Function
Bit 0	MYBERR+	Bus Error occurring during WDC's bus mastership
Bit 1	PIOINM+	Output Data Register empty (See Adapter Data Phase and Command Phase)
Bit 2	OPCOMP+	Operation Complete (See Adapter Status Phase)
Bit 3	PIOUTF+	Input Data Register Full (See Adapter Status Phase and Message Phase)
Bit 4	SRESET+	SCSI bus in Reset state
Bit 5	MSG+	SCSI bus in Message Phase
Bit 6	BUSY+	SCSI bus BUSY
Bit 7	CMD+	SCSI bus in Command, Status or Message Phase

- **Address CC000A** - Host Selects WDC

  The host selects the Controller by writing to this address; the presence of data is indicated by a logical "1". Refer to the paragraphs that follow concerning bus transaction phases.

- **Address CC000B** - Host Read Input Register

  During the Information Transfer Phase, the host reads the Input Register to determine if the register is full or if data is expected. Refer to the paragraphs that follow concerning bus transaction phases.

- **Address CC000C** - Host Clears Bus Error Latch

  The Bus Error signal is latched if it occurs during WDC bus mastership. All DMA transfers are halted and control of the SCSI bus is released. The latch remains set TRUE until cleared by the host. If interrupts are enabled, a host interrupt is generated.

3.2.2 WDC Transaction

Communication between the BOSS IX system and the WDC is controlled by a six-phase transaction which is initiated by the host. The transaction is initiated when the host selects the WDC. Upon being selected, the WDC contends for bus mastership with the other DMAs connected to the host. Upon winning the arbitration, the WDC takes control of the SCSI bus and issues appropriate interrupt requests to the host. The host responds accordingly, and the six-phase transaction begins.

The host may cancel a transaction that has started by sending SRST to the WDC; this will initialize the WDC and put the SCSI bus into its Bus Free status. The entire six-phase transaction within the WDC is controlled by a group of Programmed Logic Array (PAL) devices.

The detailed operation of the PALs for the single-board WDC is slightly different from that for the two-board WDC; consequently, the PAL state diagrams, operation timing diagrams and logic diagrams, as well as parts lists for each WDC are continued in separate portions of this manual: Appendix A for the single-board WDC, and Appendix B for the two-board WDC. The following is a summary of the six-phase transaction.

- **Bus Free Phase:** This Phase occurs when the WDC is initialized or reset, indicating a NOT BUSY condition (Status Bit 6, BUSY = 0 = FALSE). All control lines are deasserted.

- **Selection Phase:** Before a command is initiated, the BOSS IX system monitors Status Bit 6, BUSY, for FALSE (high) condition; if high, BOSS IX system issues SEL- signal and begins writing DB0- bits to Address CC000A (data present = 1).

- **Command Phase:** With the WDC selected, Status Bit 7 (CMD) is asserted; the I/O line is asserted (high) with Status Bit 1 (PIOINM). The BOSS IX system sends the WDC a series of Command words, byte by byte. The Command words are defined by the Command Description Block (CDB) format to be described later. Bit 1 (PIOINM) goes TRUE (high) when the Adapter Output Register is empty and FALSE when full. Command bytes cannot be sent via DMA.

- **Information Transfer Phase:** Depending upon the CDB values, data may be transferred between the BOSS IX system and the WDC either via DMA or via programmed I/O, as discussed in the paragraphs that follow.

  1. SEQEN+ (Control Register Bit 3) TRUE: data transferred via DMA. Data transfer takes place at a Microprocessor-controlled rate.

  2. SEQEN+ FALSE; CMD (Status Bit 7) held TRUE (asserted): data is transferred via programmed I/O, as follows:

     - When PIOINM (Status Bit 1) is asserted (Input Buffer full), host writes data to Output Register Address CC0008.

     - When PIOUTF (Status Bit 3) is asserted (Output Buffer full), host reads data from Input Register Address CC000B.

- **Status Phase:** Status Phase is entered when CMD (Status Bit 7) and PIOUTF (Status Bit 3) and OPCOMP (Status Bit 2) are asserted. If host interrupts are enabled (INTEN, Control Register Bit 2 is TRUE), the host is interrupted; if not, OPCOMP is monitored by the host to determine command completion status. (See paragraph 3.2.3 for a discussion of the Completion Status Bytes.)

- **Message Phase:** The Message Phase occurs after the Status Phase is read. PIOUTF (Status Bit 2), MSG (Status Bit 5) and CMD (Status Bit 7) are all asserted. The host reads the Message byte (which is always zero and has no significance) and causes the WDC to return to the Bus Free Phase (all control lines deasserted). To initiate another command, the WDC must be again selected and the six-phased transaction is repeated.

3.2.3 Completion Status Byte

The Completion Status Byte indicates the results of the current transaction; it is read by the host during the Status Phase. The structure and the significance of the Completion Status Byte are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	Reserved				BUSY	EQUAL	CHECK	Resvd

Bits<7..4> **Reserved** - Always zero

Bit<3> **BUSY** WDC is not ready and is unable to accept a command from BOSS IX system. BUSY is always sent when a CHECK status (Bit 1 set) is returned.

Bit<2> **EQUAL** When set, indicates Search Complete.

Bit<1> **CHECK** When set, indicates a WDC error and that SENSE data is available. To determine the type of error that occurred, the host issues a REQUEST SENSE command, which causes the appropriate Command Error Code to be issued (refer to paragraph 3.2.4).

Bit<0> **Reserved** - Always zero

3.2.4 Error Sensing

Setting the CHECK bit in the Completion Status Byte causes SENSE data to be made available for return to the BOSS IX system in response to a REQUEST SENSE Command. BUSY is returned to the host. The SENSE data is saved by the WDC until requested, and is cleared when the host acknowledges receipt of the CHECK data.

In the REQUEST SENSE Command structure, the Number of Blocks field (Byte 04) specifies the number of bytes allocated by the host for returned SENSE. Byte values of 00 to 03 default to 04.

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	1	1
01	Logical Unit No.			Reserved				
02	Reserved							
03	Reserved							
04	Number of Bytes							
05	Control Byte (Reserved)							

3.2.5 Sense Byte Structure

The structure and significance of the bits in the SENSE byte which is returned to the BOSS IX system in response to the REQUEST SENSE Command is shown below. In the SENSE byte, the Address Valid bit (Byte 00<7>) indicates that the Logical Address bytes contain valid information. The Error Class field value defines whether the error is drive-related (00), data-related (01) or system-related (02).

BYTE/BIT	7	6	5	4	3	2	1	0
00	AdVal	Error Class			Error Code			
01	Reserved			(MSB)	Logical Block Address			
02	Logical Block Address							
03	Logical Block Address							

3.2.6 Error Codes

3.2.6.1 Class 00 Error Codes

Class 00 Error Codes are drive-related errors. The codes are as follows:

00	NO SENSE	03	WRITE FAULT
01	NO INDEX SIGNAL	04	DRIVE NOT READY
02	NO SEEK COMPLETE	06	NO TRACK ZERO

3.2.6.2 Class 01 Error Codes

Class 01 Error Codes are (target) data-related errors. The codes are as follows:

10	I.D. CRC ERROR	18	DATA CHECK IN NO RETRY MODE
11	UNCORRECTABLE DATA ERROR	19	ECC ERROR DURING VERIFY
12	I.D. ADDRESS MARK NOT FOUND	1A	INTERLEAVE ERROR
13	DATA ADDRESS MARK NOT FOUND	1B	NOT ASSIGNED
14	RECORD NOT FOUND	1C	UNFORMATTED OR BAD FORMAT ON DRIVE
15	SEEK ERROR	1D	SELF TEST FAILED
16	NOT ASSIGNED	1E	DEFECTIVE TRACK (MEDIA ERRORS)
17	NOT ASSIGNED	1F	NOT ASSIGNED

3.2.6.3 Class 02 Error Codes

Class 02 Error Codes are system-related errors. The codes are as follows:

20	INVALID COMMAND	23	VOLUME OVERFLOW
21	ILLEGAL BLOCK ADDRESS	24	BAD ARGUMENT
22	NOT ASSIGNED	25	INVALID LOGICAL UNIT NUMBER

26-2F NOT ASSIGNED

3.2.7 Power UP/Reset

When power is applied, the WDC enters a 10- to 20-second (10 seconds per drive) power-up sequence. Once the drive(s) come(s) ready, the WDC reads driver parameter information for Track 0, including block size and drive type data. If a Software Reset is received, the power up sequence is the same, except the 20-second timeout is reduced to 200 milliseconds, since the drives are assumed to be at speed. The drive parameter information is not read if a drive is not ready after timeout; instead, a WDC command must be issued to that unit (excluding the TEST UNIT READY command) to initiate reading other drive parameters.

In a cold start, the WDC recalibrates the head to Track 0 by introducing a 3-Head Offset and verifying a Head Seek back to Track 0. The drive parameter information for that unit is then saved in the WDC.

If the drive is unformatted or the format data is not recognized by the WDC, the WDC causes a "blown format" bit in BOSS IX on board system memory to be set; the (Power Up) sequence is halted for that unit. If the drive format is correct, the WDC causes the drive to read the largest block address present, up through the last cylinder.

The drive is returned to Track 0, stopping in selected "zones" in each track to read the defect count in the zone. These counts are saved in the WDC and used to establish the location of target blocks on the disk during reads, writes and seeks.

During the Reset sequence, the WDC performs a series of self-diagnostics which render the WDC unavailable for use for about one second after a hardware Reset is sent. Therefore, the Reset line should be used only for initial or emergency power up, not if the disk system is "lost" or between commands. Also, if the drive is not formatted or the format is unreadable, the first command after reset (except Request Sense, Test Unit Ready, Start/Stop, Send Diagnostic or Mode Select) will show an error.

If a SENSE command is issued, the returned error code will be an error code without the 'address valid' bit (bit 7) set. The controller will NOT allow any operation that READs, WRITEs or moves the heads on a drive with a 'blown' format. Instead, any of the above operations will return an error status and an error code of 1C. The 1C code indicates that the format on this drive is bad. The drive must be formatted by the WDC to prevent this "blown format" lockout. If the drive has been formatted by a WDC and an error comes up at reset, the probable cause is the controller being unable to read the disk. The controller will make another attempt to recover the drive format information every time a read/write command is issued. The $1C_H$ error is returned only when the recovery attempt is failed.

3.2.8 Power Down/Power Fail Detect

When the WDC experiences a power failure, the Power Fail Detect (PFD) line on the BOSS IX system I/O bus is driven TRUE, and the entire WDC is Reset because PFD is logically OR'd with Reset. In addition, PFD causes Write Gate Inhibit to be asserted to prevent a Write glitch on the disk. Since the drive does not receive PFD, it must be independently capable of detecting a power failure, so that it can position the heads over the landing zone area and/or prevent erroneous writing.

3.2.9 Disk Drive Formatting

Every disk drive must be formatted by the WDC (or comparable controller) before data can be written to or read from the drive. Formatting is initiated by the Test Unit Ready command from the BOSS IX system; the WDC responds with a Status byte value of 00, or the command is repeated until the Check and Busy bytes are clear. When the 00 Status byte is received, the BOSS IX system issues Mode Select containing the necessary drive parameters, followed by a Format command to initiate the actual format. The WDC formats the disk and stores the drive parameters on the disk, so there is no need to repeat this information to the WDC with every Reset or Power Up.

3.2.10 BOSS IX system to WDC Sequencing

The BOSS IX system (host) to WDC (controller) sequencing logic is primarily implemented in PAL (Programmed Logic Array) Sequencers using combinational and sequential machine logic.

State diagrams, timing diagrams, PAL signal listings and the logic diagrams associated with the single-board WDC are contained in Appendix A; those associated with the two-board WDC are contained in Appendix B of this manual. These sources may be used when considering the detailed operation of the sequencers. Overall, the following functions are involved in BOSS IX system to WDC sequencing:

- Set and reset SCSI Output Buffer Empty status (PIOINM).
- Direct fetching of data from lower or upper byte of Data Registers for SCSI controller.
- Unpack upper and lower Status Byte of Data Register.
- Internal Bus Request to BOSS IX system interface.
- Provide diagnostic features.

BOSS IX system to WDC sequencing is significantly different when data transfer from host to controller is via DMA than when transfer is via I/O bus. The following paragraphs summarize the sequencing functions.

3.2.10.1 Output Buffer Empty Status

The Output Buffer Empty status bit (PIOINM) is set if the WDC requests a byte of data and ACKIN has not been sent to acknowledge transfer of data. PIOINM is reset when ACKIN is set to acknowledge transfer.

3.2.10.2 Direct Fetching of Data

During a data transfer sequence, SEQEN (Control Register bit 3) is used to distinguish between a DMA cycle and a programmed I/O cycle. If SEQEN is FALSE (high), data transfer is via programmed I/O; if SEQEN is TRUE (low), a DMA cycle with full handshake between BOSS IX system and WDC is initiated. Command and status bytes are always transferred by programmed I/O.

3.2.10.3 Unpacking Data Registers

During each cycle of a DMA WRITE operation, a word is transferred into the upper and lower bytes of the WDC Input Data Register. The Data Register Empty flags (UDRE = Upper; LDRE = Lower) provide status and data flow steering functions into the SASI Output Buffer. The upper byte is fetched before the lower byte.

3.2.10.4 Generating Internal Bus Requests

Generation of an internal bus request with full handshaking with the host through the EBUS interface logic is controlled primarily by the BRQIN signal in conjunction with PREFE, as follows:

- When a DMA cycle has been initiated and there has been no new DMA request (PREFET and BRQIN- are both TRUE), DMA is enabled and a bus request is initiated. The HTC (host to controller) PAL monitors the DMA cycle and causes DRBUS to signal completion, although the actual transfer of upper and lower byte data is not complete; the HTC PAL continues transferring data until data transfer is complete.

- When the upper byte data transfer is completed, UDRE goes TRUE to enable lower byte data transfer. At the same time, BRQIN goes FALSE to enable another DMA cycle. This interaction results in the possible overlap of bus request (BRQIN) with the fetching of lower byte data.

3.2.11 WDC to BOSS IX System Sequencing

WDC to BOSS IX system sequencing is similar to BOSS IX system to WDC sequencing, in that the activities are controlled primarily by PAL Sequencers. Refer to the appropriate Appendix for detailed examination of sequencer operation.

Overall, the following functions are involved with WDC to BOSS IX system sequencing operations:

- Set and reset SCSI Input Buffer empty status (PIOUTF)
- Set and reset Operation Complete status bit (OPCOMP)
- Direct fetch of data from the SASI Input Buffer into the upper or lower byte of the Data Registers
- Pack and load upper or lower byte of Data Register for transfer to host memory
- Internal bus request to BOSS IX system interface
- Provide diagnostic features

WDC to BOSS IX system sequencing is significantly different when data transfer from the controller to host is via DMA than when transfer is via I/O bus. The following paragraphs summarize the sequencing functions.

3.2.11.1 Input Buffer Empty Status

The Input Buffer Empty status bit (PIOUTF) is set if the WDC requests a byte of data and ACKOUT has not been returned to acknowledge host acceptance. PIOUTF is set for DMA mode, and when ACKOUT- goes TRUE, the host clocks data into the Input Buffer, upper bytes first. PIOUTF is reset when ACKOUT- is set, and is polled by the host to determine DMA transfer activity.

3.2.11.2 Operation Complete Status

The OPCOMP bit in the Control Register Word is set when the WDC enters the Status Phase and issues the Status Completion Byte. The BOSS IX system may accept the completion byte through the Status Register, or wait for an interrupt if interrupts are enabled.

3.2.11.3 Direct Loading of Data

Direct loading of data into the Input Data Register is accomplished in one of two ways:

- If SEQEN is FALSE, data transfer is via programmed I/O; message or data bytes are loaded from the SASI bus into the Lower Input Data Register. Command and status bytes are always transferred by programmed I/O.
- If SEQUEN is TRUE (low), a DMA cycle with full handshake between the WDC to BOSS IX system is initiated. Data is transferred from the Input Buffer, upper byte first. Loading of the lower data byte enables the next bus request; there is no overlap of bus request and loading of data.

3.2.11.4 Generating Internal Bus Requests

In a DMA cycle, an internal bus request (BRQOUT) with full handshaking is generated after both upper and lower bytes have been loaded into the Input Data Register. The CTH (controller to host) PAL monitors the DMA cycle and causes DRBUS to go FALSE to signal completion, although the actual transfer of data is not complete; the PAL continues transferring data until loading is complete.

3.2.12 Diagnostic Features

The BOSS IX system can test the WDC by appropriate READ/WRITE operations to the various I/O data registers, data buffers and data paths through the PAL Sequencers on the board. The testable areas are:

- o Interrupt Vector Register
- o Control Register
- o Status Register
- o EBUS I/O Data Register
- o SCSI Interface I/O Data Buffers
- o DMA and Interrupt Logic

3.2.12.1 Register and Buffer Tests

The registers and buffers are tested by performing a programmed WRITE to location CC0008 in the Bus Free Phase with DMA disabled. Data is routed through the Upper Output Data Register and the Output Buffer into the Input Buffer. Next, a programmed READ operation to location CC0008 is performed. Data is transferred from the Input Buffer through the Lower Input Data Register to the EBUS. The BOSS IX system monitors the results.

3.2.12.2 DMA and Interrupt Logic Tests

The DMA and Interrupt arbitration logic is tested by first initiating a bus request by doing a "dummy" programmed I/O WRITE to location CC0008 when DMA is enabled during the Bus Free Phase. The CC0008 data is loaded into the Upper BOSS IX system Transceiver, followed by the loading of the Lower BOSS IX system Transceiver. The data is then transferred sequentially through the Upper and Lower SCSI Bus Transceivers to the SCSI Bus. At the same time the Lower SCSI Bus Transceiver is being loaded, the BOSS IX system is performing a programmed I/O READ on the Upper SCSI Bus Transceiver. Next, another programmed I/O WRITE to location CC0008 is performed, which causes the above cycle to be repeated. The operation is repeated as many times as desired, with the address counters being incremented at the end of each DMA cycle.

3.3 DETAILED DESCRIPTION OF COMMAND DESCRIPTION BLOCK (CDB)

The Command Description Block (CDB) is a series of 8-bit command words which define the character of the I/O request made by the DTC to the WDC. The words are transmitted to the WDC one byte at a time; all bytes must be transmitted to complete a command. At the end of the command, the WDC returns a Completion Status Byte, which is read by the host during the Status Phase. Class 00 CDBs are 6-byte commands; Class 01 CDBs are 10-byte commands. In each class, the first byte (00) contains the Class Code and the Operation Code. Depending upon the value of this byte, the remaining 5 or 9 bytes contain the Logical Unit Number, Logical Block Address and the Number of Blocks that may be transferred under a single command. Class 01 CDBs also contain a field of Command Specific Bits.

The following definitions apply to the fields specified in Tables 3-1 and 3-2.

- **Class Code** - Can be 0 to 7; only 0 and 1 used at this time.
- **Operation Code** - 32 commands allowed for each class (00h thru 1Fh).
- **Logical Unit Number** - Up to eight devices per Controller; WDC allows only two: 00 for Drive 0 and 01 for Drive 1.
- **Logical Block Address** - Class 00 commands contain 21-bit starting block addresses.
- **Number of Blocks** - Variable number of blocks may be transferred under a single command: Class 00 = 256 blocks; 00 value defaults to maximum value.
- **Control Byte** - Last byte reserved; must be zero.

3.3.1 Class 00 Command Descriptions

Class 00 Commands are 6-byte commands which typically express Read/Write instructions. Table 3-1 shows a typical Class 00 command descriptor format.

Table 3-1. Class 00 Command Block Format

BYTE/BIT	7	6	5	4	3	2	1	0
00	Class Code			OpCode				
01	Logical Unit No.			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address							
	Number of Blocks							
05	Control Byte (Reserved)							

3.3.1.1 Class 00 Command Code Summary

Table 3-2 lists the codes that are currently used for Class 00 Commands.

Table 3-2. Class 00 Command Code Summary

OP CODE	COMMAND	OP CODE	COMMAND
00h	TEST UNIT READY	0Fh	TRANSLATE
01h	REZERO UNIT	13h	WRITE BUFFER
03h	REQUEST SENSE	14h	READ BUFFER
04h	FORMAT UNIT	15h	MODE SELECT
08h	READ	1Ah	MODE SENSE
0Ah	WRITE	1Bh	START/STOP UNIT
0Bh	SEEK	1Ch	RECEIVE DIAGNOSTIC
		1Dh	SEND DIAGNOSTIC

3.3.1.2 Test Unit Ready (Op Code 00h)

The TEST UNIT READY Command returns zero status if the requested unit is turned on and ready. If not ready, a Check condition will be set in the Completion Status Byte, and the appropriate Error Code is set in the Sense Byte, as described later. The possible Sense Errors are: Drive Not Ready (04h) and Write Fault (03h). The normal bit pattern for the TEST UNIT READY Command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0	0
01	0	0	0	Reserved				
02	Reserved							
03	Reserved							
04	Reserved							
05	Reserved							

3.3.1.3 Rezero Unit (Op Code 01h)

The REZERO UNIT Command sets the selected drive to Track 0, then sends Completion Status. Possible Sense Errors are: No Seek Complete (02h); Drive Not Ready (04h); No Track Zero (06h). The normal bit pattern for the REZERO UNIT Command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0	1
01	0	0	0	Reserved				
02	Reserved							
03	Reserved							
04	Reserved							
05	Reserved							

3.3.1.4 Request Sense (Op Code 03h)

The REQUEST SENSE Command is issued by the host when the CHECK bit is set in the Completion Status Byte which is sent to the host at the end of each Command cycle. Refer to paragraphs 3.2.4 through 3.2.6 for a discussion of the Error Sensing information exchange between the DTC and WDC which results.

3.3.1.5 Format Unit (Op Code 04h)

The FORMAT UNIT Command formats all sectors with ID and data fields in accordance with the selected interleave factor. The WDC writes from index to index the ID and data fields with a block size as specified by an immediately preceding MODE SELECT Command. If no MODE SELECT Command has been executed, the block size from the previous block data is used. On unformatted or "bad format" disks (SENSE = 1Ch following a READ Command), a MODE SELECT Command is required prior to the FORMAT UNIT Command. Unless otherwise specified in the FORMAT UNIT Command, data fields are completely written with 6Ch. The command structure and significance of the fields are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	0	1	0	0
01	Logical Unit No.			Data	Cmplt	List Format Bits		
02	Data Pattern							
03	(MSB)	Interleave						
04	Interleave							(MSB)
05	Control Byte (Reserved)							

a. **Bad Block** Field, Byte 01<4..0>: Specifies the format of the bad block list for defect skipping:

- o **Data** bit <4> is set to alert the WDC that a list of bad areas is forthcoming and that defect skipping is to take place; if bit is not set, formatting is accomplished with no user supplied data.
- o **Complete List** bit <3> is set to specify that all of the known defects on the drive are contained in the bad block list, which must be less than 1024 bytes long.

- o **Define Format** bits <2..0>, in the following combinations only (Data bit <4> = 1):

  0 0 0 = Default.
  0 1 0 = Format with data fill byte (6Ch).
  1 1 0 = Use Cyl/Head/Byte Count format in data list.
  1 1 1 = Use data pattern defined by FORMAT UNIT Byte 02.

b. **Data Pattern** Field, Byte 02<7..0>: contains the defect list whose format is established by Byte 01<2..0>, above. The list, which is limited to 1024 bytes so it can fit into the available buffer space, includes the physical coordinates of known media flaws, in ascending order of cylinder, head, and bytes from Index.

If defects are not presented to the WDC in ascending order, a Bad Argument Error (24h) is reported. The following is the defect list format:

BYTE/BIT	7	6	5	4	3	2	1	0
00	Reserved							
01	Reserved							
02	(MSB) Length of Defect List in Bytes (8N)							
03	" (LSB)							
04	(MSB) Cylinder Number of Defect #1							
05	"							
06	Cylinder Number of Defect #1 (LSB)							
07	Head Number of Defect #1							
08	(MSB) Bytes from Index							
09	"							
10	"							
11	Bytes from Index (LSB)							
8N-4 to 8N+3	Nth Defect							

c. **Interleave** Field, Bytes 03,04: The WDC does not require interleaving because of its high-speed buffer control.

3.3.1.6 Read (Op Code 08h)

The READ Command transfers to the DTC the specified number of blocks starting at the specified Logical Block Address. The WDC verifies that the Seek Address is valid and causes a Seek to the specified address. When Seek Complete occurs, the WDC reads the starting address data field into the buffer, checks ECC and begins DMA data transfer. Data transfer continues until the block count is decremented to zero. ON a data ECC error, the block is re-read up to five times before correction is attempted. Correction is done directly into the data buffer, transparent to the host. The bit pattern of the READ Command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	0	0
01	Logical Unit No.			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address (LSB)							
04	Reserved							
05	Control Byte (Reserved)							

3.3.1.7 Write (Op Code 0Ah)

The WRITE Command transfers to the target drive the specified number of blocks starting at the specified Logical Block Address. The WDC verifies that the Seek Address is valid and Causes a Seek to the specified starting block. When Seek Complete occurs, the WDC transfers the first block into its buffer and writes its buffered data and its associated ECC into the first logical sector. Subsequent data blocks are transferred as available from the FIFO buffer until the block count is decremented to zero.

The WDC also supports extended READ and WRITE Commands using the Class 01 CDB format, described later. The bit pattern of the WRITE Command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	1	0
01	Logical Unit No.			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Reserved							
05	Control Byte (Reserved)							

3.3.1.8 Seek (Op Code 0Bh)

The SEEK Command causes the selected drive to seek to the specified starting address. Immediately after the Seek pulses are issued and head motion starts, the WDC returns Completion Status. If the WDC receives another command while seek is in progress, it returns a Completion Status of BUSY; this allows the host to use the SCSI bus to do other processing while waiting for Seek Complete. The WDC uses an implied Seek on READ, WRITE and SEARCH commands, making it unnecessary to issue a SEEK command with each operation.

Whenever overlapped operations are desired, the SEEK command must be used, and INTEND0 <bit 4> or INTEND1 <bit 5> in Control Register I/O Address CC0007 must be set. Setting this bit causes the DTC to check CC0007 bit 6 (INTD 0) or 7 (INTD 1) for Seek Complete Interrupt Status before executing an RTE instruction. The appropriate interrupt status bit is reset before the overlapping interrupt is in service; the host is thus prevented from being re-interrupted by the Seek routine when it is completed. The overlapped operations feature may be used only with buffered-seek type drives (checked with the Mode Sense Command). The bit pattern of the SEEK Command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	1	1
01	Logical Unit No.			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Reserved							
05	Control Byte (Reserved)							

3.3.1.9 Translate (Op Code 0Fh)

The TRANSLATE command translates a Logical Block Address (LBA) into a physical location and returns the physical address to the DTC in a cylinder/head/bytes from Index format. If LBA is used to build a defect list for the FORMAT UNIT command, eight bytes are required. If there is a data error in the LBA field, a CHECK status is returned in Completion Status. It is then necessary to TRANSLATE the blocks before and after the targeted block to determine the location of the target block. The bit pattern of TRANSLATE is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	1	1	1	1
01	Logical Unit No.			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Reserved							
05	Control Byte (Reserved)							

3.3.1.10 Write Data Buffer (Op Code 13h)

The WRITE DATA BUFFER command is used by the host during diagnostics to fill the Input Buffer with 1K-bytes of data. The bit pattern for WRITE DATA BUFFER is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	0	0	1	1
01	Logical Unit No.			Reserved				
02	Reserved							
03	Reserved							
04	Reserved							
05	Control Byte (Reserved)							

3.3.1.11 Read Buffer RAM (Op Code 14h)

The READ BUFFER RAM command is used by the host to fill the Output Buffer with 1k-bytes of data for diagnostic purposes. Although data remains in the buffer after normal operations begin, it is undefined until overwritten with significant data. The bit pattern for the READ BUFFER RAM is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	0	1	0	0
01	Logical Unit No.			Reserved				
02	Reserved							
03	Reserved							
04	Reserved							
05	Control Byte (Reserved)							

3.3.1.12 Mode Select (Op Code 15h)

The MODE SELECT command always precedes the FORMAT UNIT command; it specifies the formatting parameters. When the SENSE byte returns a "blown format" Error Code (1Ch), MODE SELECT can be used to inform the WDC about the Drive information. The Drive should be backed up and reformatted. The bit pattern and bit significance for MODE SELECT are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	0	1	0	1
01	Logical Unit No.			Reserved				
02	Reserved							
03	Reserved							
04	Number of Bytes							
05	Control Byte (Reserved)							

Byte 04 of the MODE SELECT command specifies the number of information bytes to be passed with the command, a minimum of 12 bytes (0Ch). If Drive parameters are being specified, the count is 22 bytes (16h). The Extent Descriptor List and the Drive Parameter List are a single data block of 8 bytes and 10 bytes, respectively. Byte 04 consists of the following:

a. **Mode Select Parameter List** (4 Bytes): The first three bytes are reserved; the fourth byte specifies the length in bytes of the Extent Descriptor List (always 8 bytes in this application). The bit pattern for the Mode Select Parameter List is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	Reserved							
01	Reserved							
02	Reserved							
03	Length of Extent Descriptor List = 08h							

b. **Extent Descriptor List** (8 Bytes): Byte 00 specifies the data density of the Drive; must be zero = FM density. Bytes 01 thru 04 are zero = reserved. Bytes 5 thru 7 specify Data Block Size = 256, 512 or 1024 bytes; any other value will return a SENSE byte CHECK status with a "Bad Argument" Error Code (24h). The Extent Descriptor List bit pattern is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	Density Code							
01	Reserved							
02	Reserved							
03	Reserved							
04	Reserved							
05	(MSB)	Block Size						
06	Block Size							
07	Block Size							(LSB)

c. **Driver Parameter List** (10 Bytes): An optional feature; if present, must include all the data necessary to specify a Drive, within the limits stated. If data is not supplied or is incomplete, previously supplied values will be used if available; if not, the following default values will be used.

BYTE/BIT	7	6	5	4	3	2	1	0
00	List Format Code = 01							
01	(MSB)	Cylinder Count						
02	Cylinder Count							(LSB)
03	Data Head Count							
04	(MSB)	Reduced Write Current Cylinder						
05	Reduced Write Current Cylinder							(LSB)
06	(MSB)	Write Precompensation Cylinder						
07	Write Precompensation Cylinder							(LSB)
08	Landing Zone Position							
09	Step Pulse Output Rate Code							

- **List Format Code** = Always 01.

- **Cylinder Count** = Number of data cylinders on the Drive: Minimum=1; Maximum=2048; Default=306.

- **Data Head Count** = Number of usable data heads (numbered 0-15) Default=2; must use Reduced Write Current line to select heads numbered 8-15.

- **Reduced Write Current Cylinder** = Cylinder number beyond which the WDC asserts the Reduced Write Current line. Minimum=0; Maximum= 2047; Default=150. (See also Data Head Count description.)

- **Write Precomposition Cylinder** = Cylinder beyond which the WDC compensates for inner track bit shift; field ignored by controller; value set by jumpers JMP B and JMP C, as follows:

  Pos 1C-2C: Wrt Precomp Cyl = Red Wrt Curr Cyl
  (Cannot be used for Drives with more than 8 heads)
  Pos 1A-2A: Wrt Precomp always off.
  Pos 1B-2B: Wrt Precomp always on.

- **Landing Zone Position** = Used with START/STOP command to indicate the direction and number of cylinders from the last (or first) data cylinder to the shipping position. MSB=0=Landing Zone outside highest track; MSB=1=Landing Zone outside Track 0; Bits <6..0> give the number of cylinders. Default=0 (land on highest, innermost track).

- **Step Pulse Output Rate Code** = Timing of Seek steps: 00=Non Buffered Seek--3.0 msec rate (per ST-506); 01=Buffered Seek--28 usec rate (per ST-412); 02=Buffered Seek--12 usec rate.

3.3.1.13 Mode Sense (Op Code 1Ah)

The MODE SENSE command is used to interrogate the Device Parameter table (paragraph 3.3.1.12) to determine the specific characteristics of the attached Disk Drive(s). If the Drive was not formatted by the WDC, a Blown Format Error (1Ch) will be returned. The bit pattern and significance of MODE SENSE are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	1	0	1	0
01	Logical Unit No.			Reserved				
02	Reserved							
03	Reserved							
04	Number of Bytes Returned							
05	Control Byte (Reserved)							

Byte 04 of the MODE SENSE command specifies the number of data bytes to be returned from the command, a minimum of 12 bytes (0Ch). If Drive parameters are being specified, the count is 22 bytes (16h). The Parameter List, Extent Descriptor List and the Drive Parameter List (if requested) are used here in the same way as they are used for MODE SELECT (paragraph 3.3.1.12).

3.3.1.14 Start/Stop (Op Code 1Bh)

The START/STOP command is used on drives with a designated shipping or landing zone. A STOP command positions the head to the Landing Zone Position designated by the Mode Parameter List in the MODE SELECT command. If the command is START, bit Byte 04<1> must be set; otherwise it is a STOP command. The bit pattern for the START/STOP command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	1	0	1	1
01	Logical Unit No.			Reserved				
02	Reserved							
03	Reserved							
04	Reserved							St/Stp
05	Control Byte (Reserved)							

3.3.1.15 Receive Diagnostic Result (Op Code 1Ch)

The RECEIVE DIAGNOSTIC RESULT command sends analysis data to the host immediately after completion of a SEND DIAGNOSTIC command which initiated the dump. The bit pattern and significance of the RECEIVE DIAGNOSTIC RESULT command are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	1	1	0	0
01	Logical Unit No.			Reserved				
02	Reserved							
03	(MSB)	Data Length						
04	Data Length							(LSB)
05	Control Byte (Reserved)							

Dump data sent to the Input Data Buffer is formatted as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	(MSB)	Data Block Length (=0104h)						
01		Data Block Length						(LSB)
02	(MSB)	Starting Address of Dump						
03		Starting Address of Dump						(LSB)
04	Dumped Data (xx00)							
103	Dumped Data (xxFF)							

3.3.1.16 Send Diagnostic (Op Code 1Dh)

The SEND DIAGNOSTIC command sends data to the WDC to specify diagnostic tests for the WDC and peripheral units. The bit pattern and significance of the SEND DIAGNOSTIC command are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	1	1	0	1
01	Logical Unit No.			Reserved				
02	Reserved							
03	(MSB)	Data Length						
04	Data Length							(LSB)
05	Control Byte (Reserved)							

a. **Data Length** Field, Byte 03: Specifies the length of the data to be sent. Length must be a minimum of four bytes long, and equal to the length of the data block to be passed to the WDC; if the specified length is longer than needed, the excess is ignored. The bit pattern and significance of the data field are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	Diagnostic Specifier							
01	Diagnostic Option or Coded Release Level							
02	Low Byte of Patch Starting Address or Qualifier							
03	Patch Data Length (00=100h) (N) or Reserved							
04	Optional Patch Data							
N+3	Optional Patch Data							

b. **Diagnostic Specifier**, Byte 00 = The specific function being requested. Patch options 63h and 64h require a data block greater than 4 bytes: 60h - Re-initialize Drive
61h - Dump Hardware Area (4000-40FF)
62h - Dump RAM (8000-80FF)
63h - Patch Hardware Area
64h - Patch RAM
65h - Set Read Error Handling Options

c. **Diagnostic Option or Coded Release Level**, Byte 01 = The subtest or qualifiers specific to the test selected by Byte 00; not checked if the 65h option code is specified.

Low Byte of Patch Starting Address, Byte 02 = Starting address in RAM or the memory-mapped registers to be patched; high byte is implicit in the specified diagnostic (Note: A Patch RAM operation with a third byte of A1h will overwrite an area of RAM starting with 80A1h.)

Patch Data Length, Byte 03 = Number of bytes to be overwritten (from 1 to 256 bytes); 0 = 256.

d. **ECC Options** Field, Byte 02: Specifies the actions to take place upon encountering a ECC check of Option 65h is selected for the Logical Unit Number addressed by the command. Default state is established by WDC Reset and remain in effect until next Reset.

e. **Set Read Error Handling Options** (Data Block Option Byte 65h):

Value 00 = Selects default options where a correctable error is corrected without comment and all data transferred without CHECK status. If the error is not correctable, the WDC transfers the uncorrected data and set CHECK status with an Error Code of 91h. The Valid Address is that of the bad block.

Value 01 = Report all corrections and stop. A correctable error will be corrected and the data transferred, but the operations will stop with a CHECK status and Error Code of 98h. An uncorrectable error is handled as in 00, above.

Value 02 = Do not correct. All ECC errors will be treated as uncorrectable except that the Error Code is set to 98h.

3.3.2 Class 01 Commands

Class 01 Commands are 10-byte commands that express additional Read/Write instructions, and Verify and Search instructions.

3.3.2.1 CDB Class 01 Command Code Summary

Table 3-3 lists the codes that are currently used for CDB Class 01 commands.

Table 3-3. CDB Class 01 Command Code Summary

OP CODE	COMMAND	OP CODE	COMMAND
25	READ CAPACITY	2E	WRITE AND VERIFY
28	READ	2F	VERIFY
2A	WRITE	31	SEARCH DATA EQUAL

3.3.2.2 CDB Class 01 Command Block Format

Table 3-4 shows a typical Class 01 command descriptor format.

Table 3-4. Class 01 Command Block Format

BYTE/BIT	7	6	5	4	3	2	1	0
00	Class Code			OpCode				
01	Logical Unit No.			Command Specific Bits				
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	Reserved							
07	Number of Blocks							
08	Number of Blocks							
09	Control Byte (Reserved)							

3.3.2.3 Read Capacity (Op Code 25h)

If CDB Class 01 Byte 08 is 00h, the READ CAPACITY command will return the address of the last block on the unit (a starting address block is not necessary). If Byte 08 is 01h, the READ CAPACITY command will return the address of the block (after the specified starting address) at which a substantial delay in data transfer will be encountered (such as a cylinder boundary. The block address and size of the data to be read are specified in the eight bytes (4 bytes for Block Address; 4 bytes for Block Size in bytes) of the Data Field returned as a result. Any byte value other than 00h or 01h will return a CHECK status with an Error Code of 24h (Invalid Argument). The bit pattern for the READ CAPACITY command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	1	0	0	1	0	1
01	Logical Unit No.			Reserved				(Rel Add)
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	Reserved							
07	Reserved							
08	Full or Partial Media Indicator							
09	Control Byte (Reserved)							

3.3.2.4 Read (Op Code 28h)

The READ command for Class 01 operations is the same as for Class 00 operations, described in paragraph 3.3.1.6.

3.3.2.5 Write (Op Code 2A)

The WRITE command for Class 01 operations is the same as for Class 00 operations, described in paragraph 3.3.1.7.

3.3.2.6 Write and Verify (Op Code 2Eh)

The WRITE AND VERIFY command for Class 01 operations is similar to the WRITE function for Class 00, in that data is written in the specified number of blocks (64K for Class 01; 256 for Class 00). In this command, the written data is then verified block by block. No data is transferred to the host; hence, correctable data checks are treated the same as uncorrectable data checks. The bit pattern for the WRITE AND VERIFY command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	1	0	1	1	1	0
01	Logical Unit No.			Reserved				
02	(MSB)	Logical Block Address						
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved							
07	Number of Blocks							
08	Number of Blocks							
09	Control Byte (Reserved)							

3.3.2.7 Verify (Op Code 2Fh)

The VERIFY command is similar to the WRITE AND VERIFY command (Op Code 2Eh), except that VERIFY checks the ECC of an already existing set of data blocks. It is up to the host to provide data for rewriting and correcting if an error is detected. The bit pattern for VERIFY is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	1	0	1	1	1	1
01	Logical Unit No.			Reserved				
02	(MSB)	Logical Block Address						
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved							
07	Number of Blocks							
08	Number of Blocks							
09	Control Byte (Reserved)							

3.3.2.8 Search Data Equal (Op Code 31h)

The SEARCH DATA EQUAL command provides for a search and compare-on-equal of any data on the disk, by using indexed access methods for rapidly searching for record key fields. When a SEARCH is satisfied, it will terminate with a Condition Met Status.

A REQUEST SENSE command can then be issued to determine the block address of the matching record, and reported as follows:

- o An EQUAL setting of the SENSE byte will be reported.
- o The Address Valid bit in the SENSE byte will be set (= 1).
- o The address of the block containing the first matching record will be reported in the Information Bytes in the SENSE byte.

Following an unsuccessful SEARCH (terminating in an inequality), the following is reported:

- o A Error Code of 00 (NO SENSE) is sent, provided there are no other errors.
- o The Address Valid bit in the SENSE byte is not set (= 0)

The bit pattern and significance of the SEARCH DATA EQUAL command are as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	0	0	1	1	0	0	0	1
01	Logical Unit No.			Invrt	Reserved			
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address (LSB)							
06	Reserved							
07	Number of Blocks							
08	Number of Blocks							
09	Control Byte (Reserved)							

a. **Invert**, Byte 01<4> = Inverts the sense of the search comparison operation. With Invert ON, the first block not-equal will return a "matching" response; also, SEARCH DATA HIGH and SEARCH DATA LOW returns would be reversed.

b. The argument following a SEARCH command is as follows:

BYTE/BIT	7	6	5	4	3	2	1	0
00	(MSB)			Record Size				
01				Record Size				
02				Record Size				
03				Record Size				(LSB)
04	(MSB)			First Record Offset				
05				First Record Offset				
06				First Record Offset				
07				First Record Offset				(LSB)
08	(MSB)			Number of Records				
09				Number of Records				
10				Number of Records				
11				Number of Records				(LSB)
12	(MSB)			Search Argument Length				
13				Search Argument Length				(LSB)
14	(MSB)			Search Field Displacement				
15				Search Field Displacement				
16				Search Field Displacement				
17				Search Field Displacement				(LSB)
18	(MSB)			Pattern Length				
19				Pattern Length				(LSB)
20	(MSB)			Data Pattern				
M+19	(MSB)			Data Pattern				(LSB)

- **Record Size** Field, Bytes 00-03 = Bytes specified must equal blocksize or zero (the format block size).

- **First Record Offset** Field, Bytes 04-07 = Field must be zero.

- **Number of Records** Field, Bytes 08-11 = Number of blocks must be more than zero and equal to or less than the number of blocks specified in the SEARCH command. SEARCH terminates upon a match or when the specified block size is reached.

- **Search Argument Length** Field, Bytes 12-13 = Number of bytes in the SEARCH argument; must = pattern length + 6.

- **Search Field Displacement** Field, Bytes 14-17 = Must be zero.

- **Pattern Length** Field, Bytes 18-19 = Number of bytes specified in the following Data Pattern to be compared with an equal size field in each record.

- **Data Pattern** Field, Bytes 20-M+19 = Variable length field of M bytes, where M = block size.

SECTION 4

MAINTENANCE

4.1 PREVENTIVE MAINTENANCE

Maintenance of the WDC consists of general cleaning, which should be accomplished along with scheduled maintenance on the host system. Cleaning of the WDC is done in the following manner:

CAUTION

Do not use abrasive cleaners and chemical cleaning agents that contain acetone, toluene, xylene, or benzene. These cleaners may cause equipment damage that requires major repair. ESD sensitivity requires proper handling of boards.

1. Use a soft bristle brush to clean dust from the surface of the printed circuit board.

2. Use a lint-free cloth dampened with a solution of 90 percent isopropyl alcohol to clean non-electrical surfaces.

4.2 CORRECTIVE MAINTENANCE

The following paragraphs describe power-up initialization and self-test, and the system diagnostics for the WDC. Failure of the self-tests or system diagnostics requires that the WDC be repaired using the maintenance data furnished in Appendix A (single-board WDC) and Appendix B (two-board WDC).

Refer to Section 2 for descriptions and pinouts of the one- and two-board WDC interfaces.

4.2.1 Power-Up Initialization and Self-Test

Upon power-up or any reset, WDC firmware performs a basic test of hardware which is crucial to correct operation of the controller. Memory bus accesses to on-board buffer RAM will be disabled from the time the reset occurs until successful completion of all of the self-tests.

In each test, the firmware does a loop on the section of the test that failed, from the start of the test to the point at which an error was detected. The following logic is tested at power up:

1. Microprocessor ALU, Registers, and Status Lines
2. Adapter Section Control Logic, Arbitration Logic and Status Registers
3. SCSI Transceivers and Latches
4. Winchester and Bus Controllers and Buffers

The WDC self-test sequence is performed during the reset phase (approximately one second long) of a cold start (or emergency) power-up sequence. If the connected drive(s) is (are) not ready after the 20-second initialization timeout, the drive parameter information is not read. Failure of the self-tests causes the "Self-Test Failed" bit in a Class 01 Error Code to be set.

4.2.2 System Diagnostics

The WDC can be tested by the BOSS IX system by performing appropriate READ/WRITE operations on the various I/O data registers, data buffers and data paths in the WDC. Verify that the jumper and switch connections are as specified in Section 2 of this manual.

4.2.2.1 Register and Buffer Tests

These tests are executed by performing a programmed WRITE to location CC0008 in the Bus Free Phase with DMA disabled. Data is routed through the Upper Output Data Register and the Output Buffer into the Input Buffer. Next, a programmed READ operation to location CC0008 is performed. Data is transferred from the Input Buffer through the Lower Input Data Register to the EBUS. The BOSS IX system monitors the results.

4.2.2.2 DMA and Interrupt Logic Tests

The DMA and Interrupt arbitration logic is tested by first initiating a bus request by doing a "dummy" programmed I/O WRITE to location CC0008 when DMA is enabled during the Bus Free Phase. The CC00008 data is loaded into the Upper BOSS IX system Transceiver, followed by the loading of the Lower BOSS IX system Transceiver. The data is then transferred sequentially through the Upper and Lower SCSI Bus Transceivers to the SCSI Bus. At the same time the Lower SCSI Bus Transceiver is being loaded, the BOSS IX system is performing a programmed I/O READ on the Upper SCSI Bus Transceiver. Next, another programmed I/O WRITE to location CC0008 is performed, which causes the above cycle to be repeated. The operation is repeated as many times as desired, with the address counters being incremented at the end of each DMA cycle.

4.2.3 WDC Adjustments

Following a WDC repair procedure, the WDC Data Separator must be adjusted as described in the paragraphs that follow.

4.2.3.1 Test Equipment Required

The recommended test equipment is as follows:

a. 100 MHz dual channel oscilloscope (Tektronix 465 or equivalent)
b. 50 MHz frequency counter
c. 50 MHz function generator
d. +/-0.5% DUM
e. BOSS IX System to power up and reset the WDC board

4.2.3.2 Data Separator Adjustment

1. Verify that the jumper and switch setitngs are as specified in Section 2 of this manual.

2. Apply power to the WDC board.

3. Reset the WDC board through a manual hard reset or soft reset. The soft reset can be executed by loading WDAFS and using command "CC"

4. Provide a TTL signal at pin 7C-10 with a period fo 400 ns. The duty cycle can be approximately 50%.

5. Adjust pot R32 for a positive pulse width of 250 ns ±5% at pin 7C-5/TP11.

6. Ground pin 6C-2.

7. Adjust R19 for a VCO frequency of 10 MHz ±1% at TP3. Use a counter for this measurement.

8. Remove ground from 6C-2.

NOTES

SECTION 5

REMOVAL/REPLACEMENT

There are no specific removal/replacement procedures for the WDC. The PCBA is removed the same as any other PCBA. When installing the WDC, observe the correct jumper and DIP switch settings and the correct card placement in accordance with instructions in Section 2 of this manual.

NOTES

APPENDIX A

SINGLE-BOARD WDC MAINTENANCE AIDS

The following Programmed Logic Array (PAL) information, interface data, parts list data and logic diagrams for the single-board WDC, part number 903496 are provided to aid in clarifying the operation of the WDC and assist in the maintenance of the PCBA:

NOTE

The PAL state diagrams and equations in this appendix are provided for reference purposes only and will not be maintained.

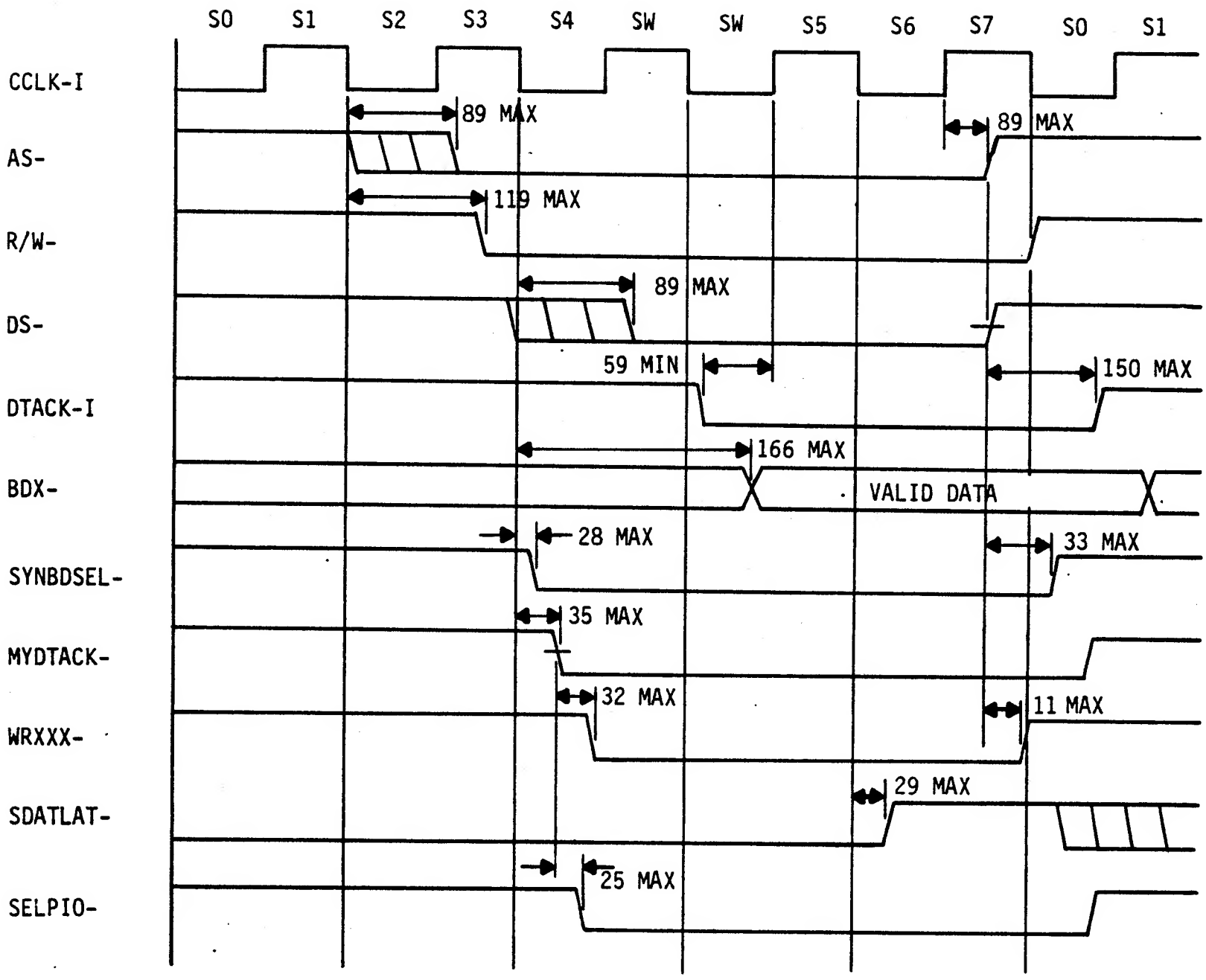


Figure A-1. BOSS IX System WRITE Timing Diagram

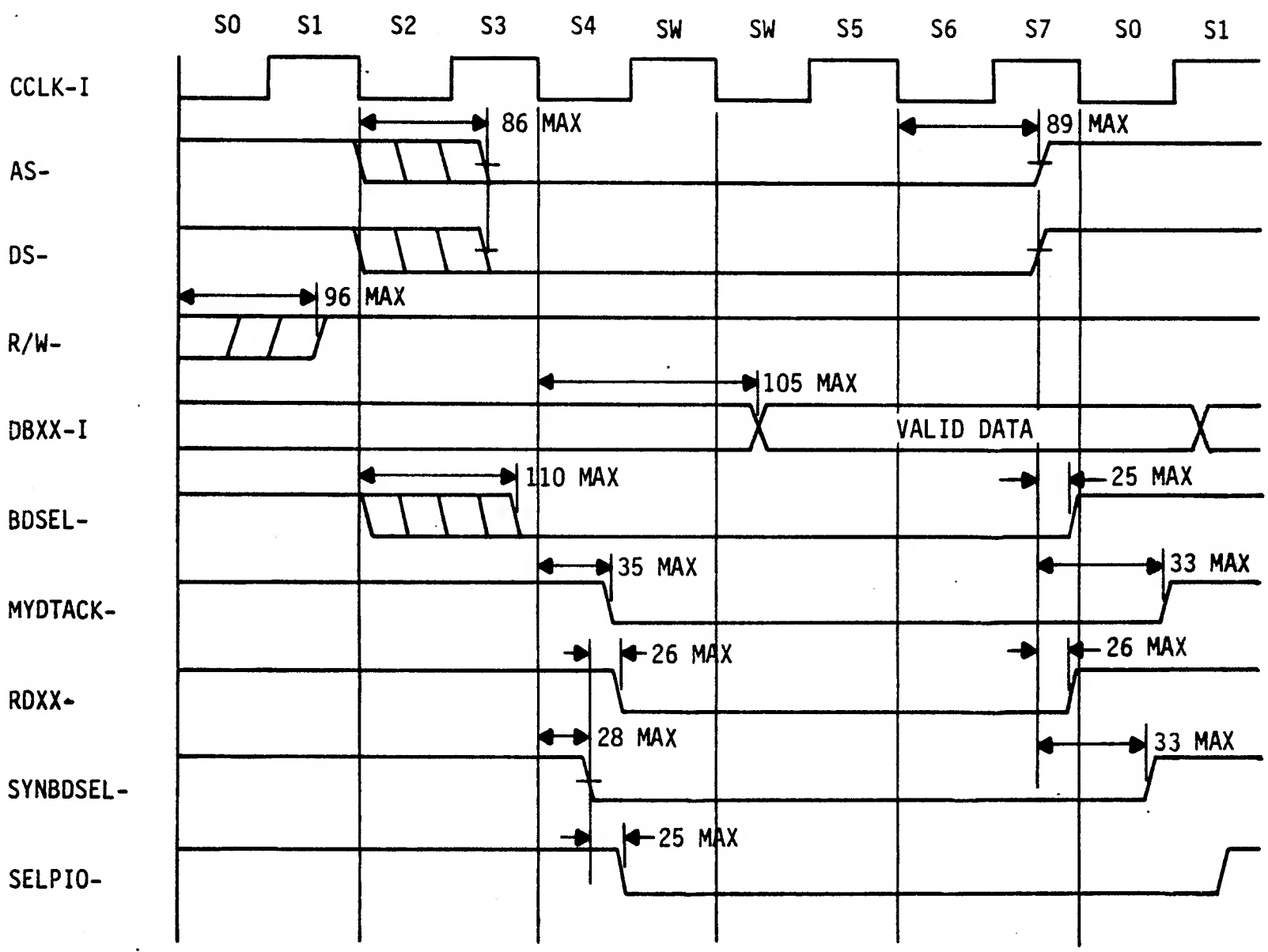


Figure A-2. BOSS IX System READ Timing Diagram

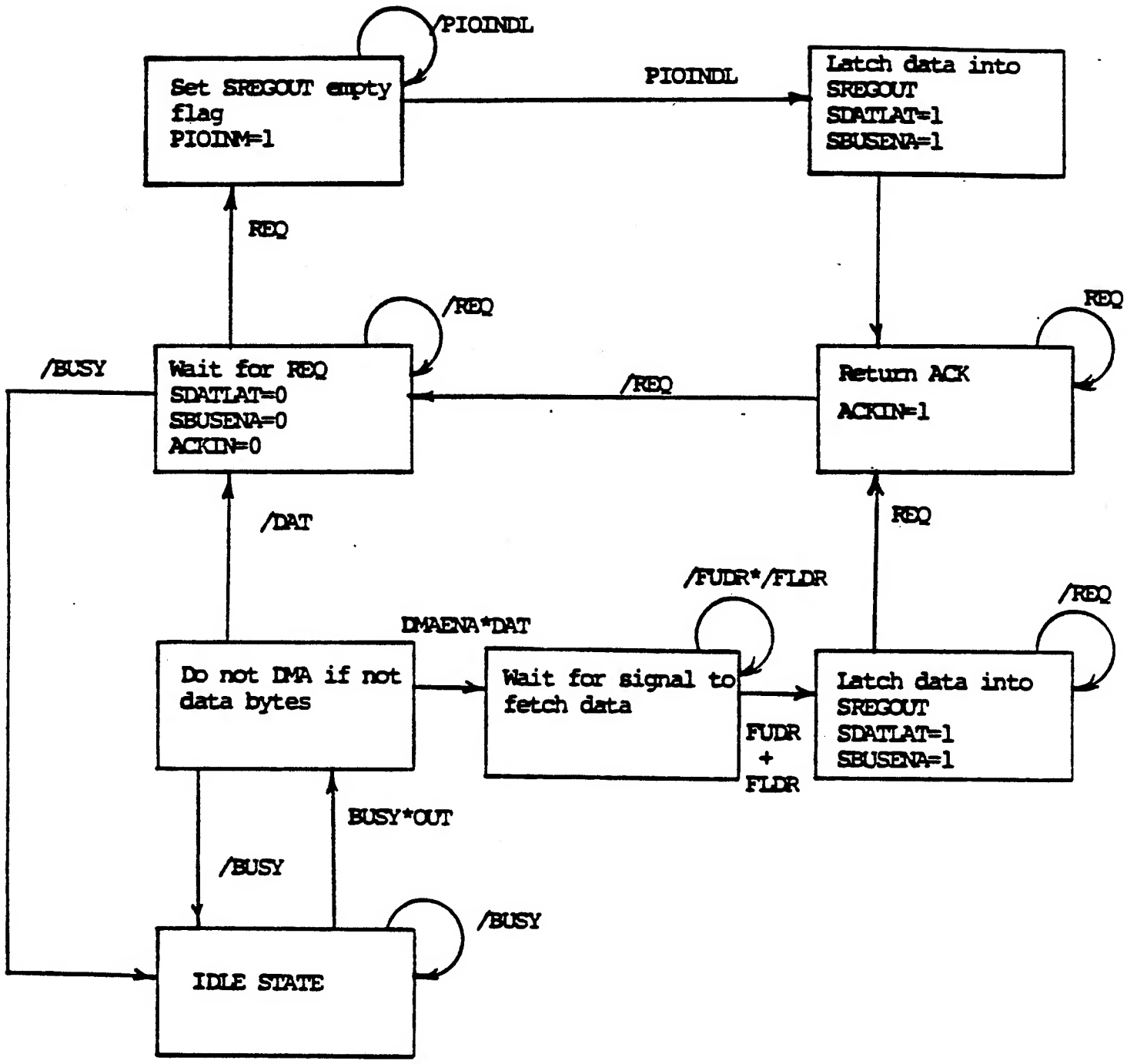


Figure A-3. BOSS IX System to WDC Programmed I/O PAL State Diagram

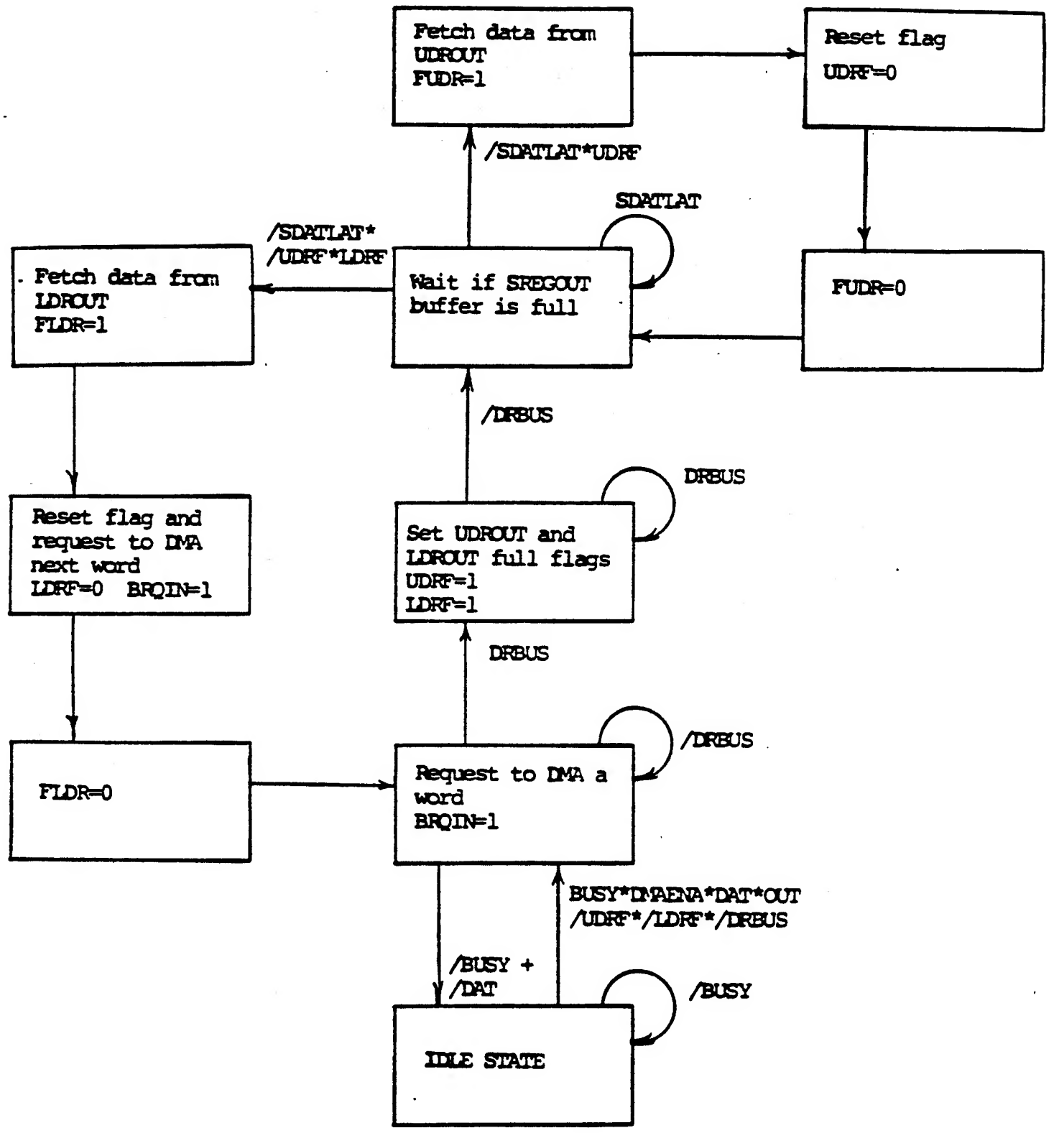


Figure A-4. WDC to BOSS IX System Programmed DMA PAL State Diagram

Table A-1. BOSS IX to Controller PAL Signal Listing

```
CCLK    /DMAENA   /DRBUS    LUDR      /PIOOUT    OUT       /PIOINDL   /LLDR   /REQ
/BUSY   DAT       GND       ENB       /SDATLAT   /SBUSENA  /UDRF      /FLDR   /LDRF
/ACKIN  /BRQIN    /FUDR     /PIOINM   /HOSTPIO   VCC
```

```
ACKOUT      := RQU * OUT * SATLAT * PIOINM
             + ACKOUT * REQ
             = DMAENA * DAT * SDATLAT * REQ * OUT

BRQIN       := DMAENA * DAT * REQ * OUT * /UDRF * /LDRF * BUSY * /DRBUS
             + FLDR * /DRBUS * BUSY
             + BRQIN * /DRBUS * DMAENA
             + DMAENA * /BUSY * PIONDL

FUDR        := UDRF * /SDATLAT * DMAENA * DAT * BUSY * OUT * /DRBUS * /HOSTPIO
             + UDRF * LDRF * /BUSY * /DRBUS * /SDATLAT

FLDR        := /UDRF * LDRF * /SDATLAT * DMAENA * DAT * BUSY * OUT * /DRBUS
               * HOSTPIO
             + /UDRF * LDRF * /DRBUS * /BUSY * /SDATLAT

PIOINM       = REQ * OUT * /ACKIN

LDRF        := DMAENA * DAT * OUT * DRBUS * BUSY
             + LDRF * /FLDR * DAT * BUSY
             + DRBUS * /BUSY
             + LDRF * /FLDR * /BUSY

VDRF        := DMAENA * DAT * OUT * DRBUS * BUSY
             + UDRF * /FUDR * DAT * BUSY
             + DRBUS * /BUSY
             + UDRF * /FUDR * /BUSY

SBUSENA     := REQ * OUT * BUSY * SDATLAT
             + DMAENA * DAT * OUT * BUSY * SDATLAT
             + FLDR * /BUSY
             + PIOINDL * /BUSY
             + LLDR
             + LUDR
```

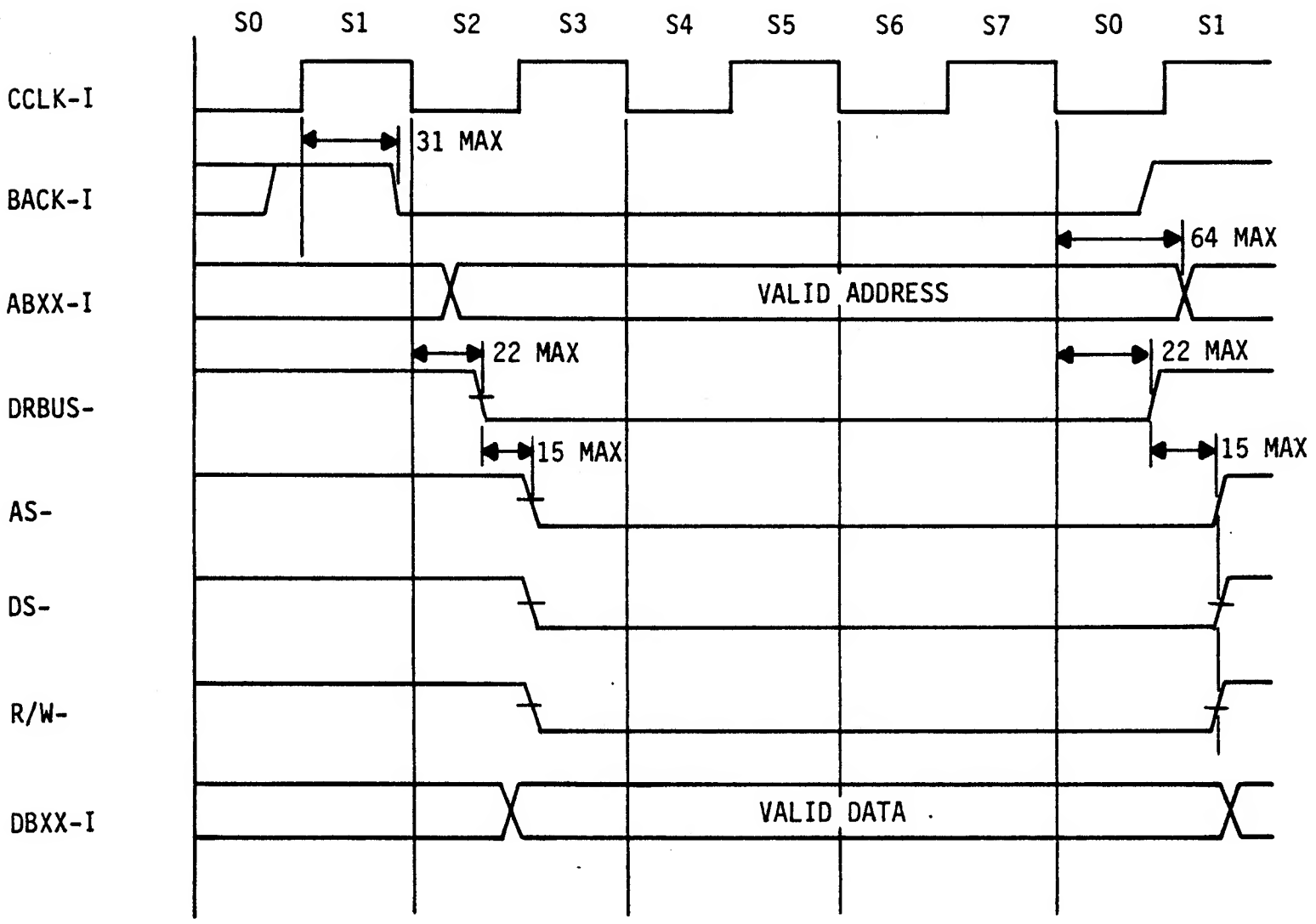


Figure A-5. DMA WRITE Operation Timing Diagram

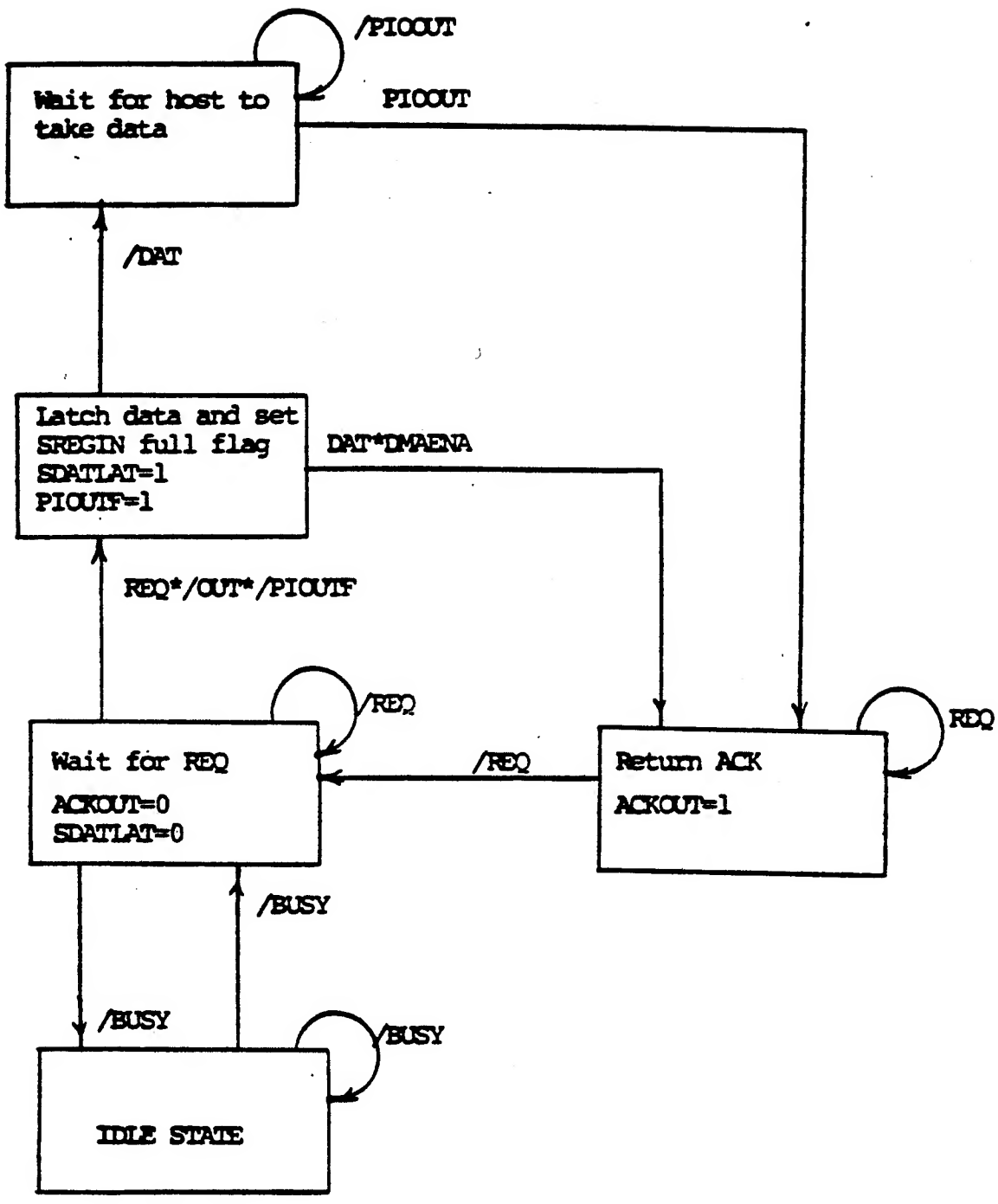


Figure A-6. WDC to BOSS IX System Programmed I/O PAL State Diagram

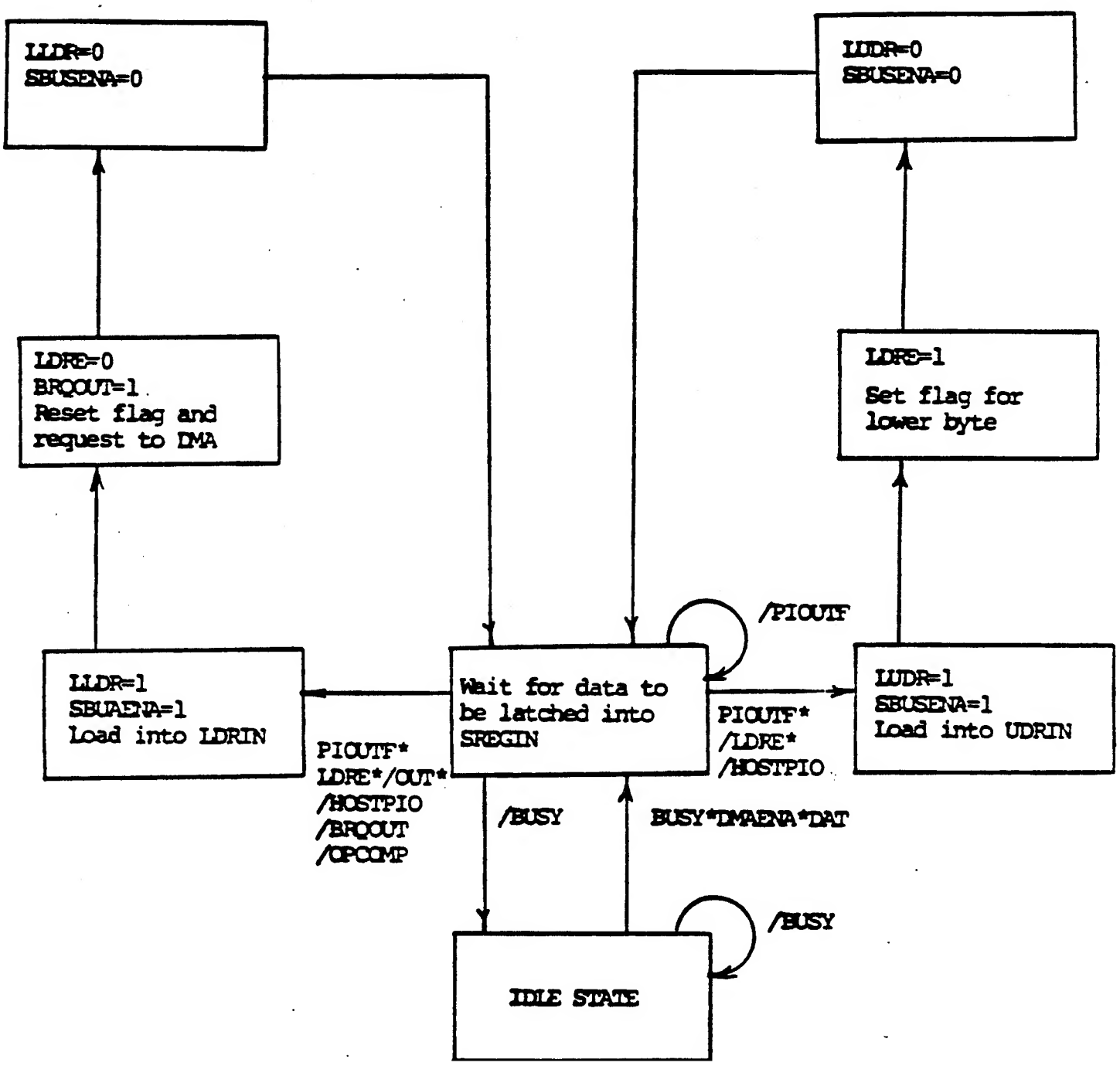


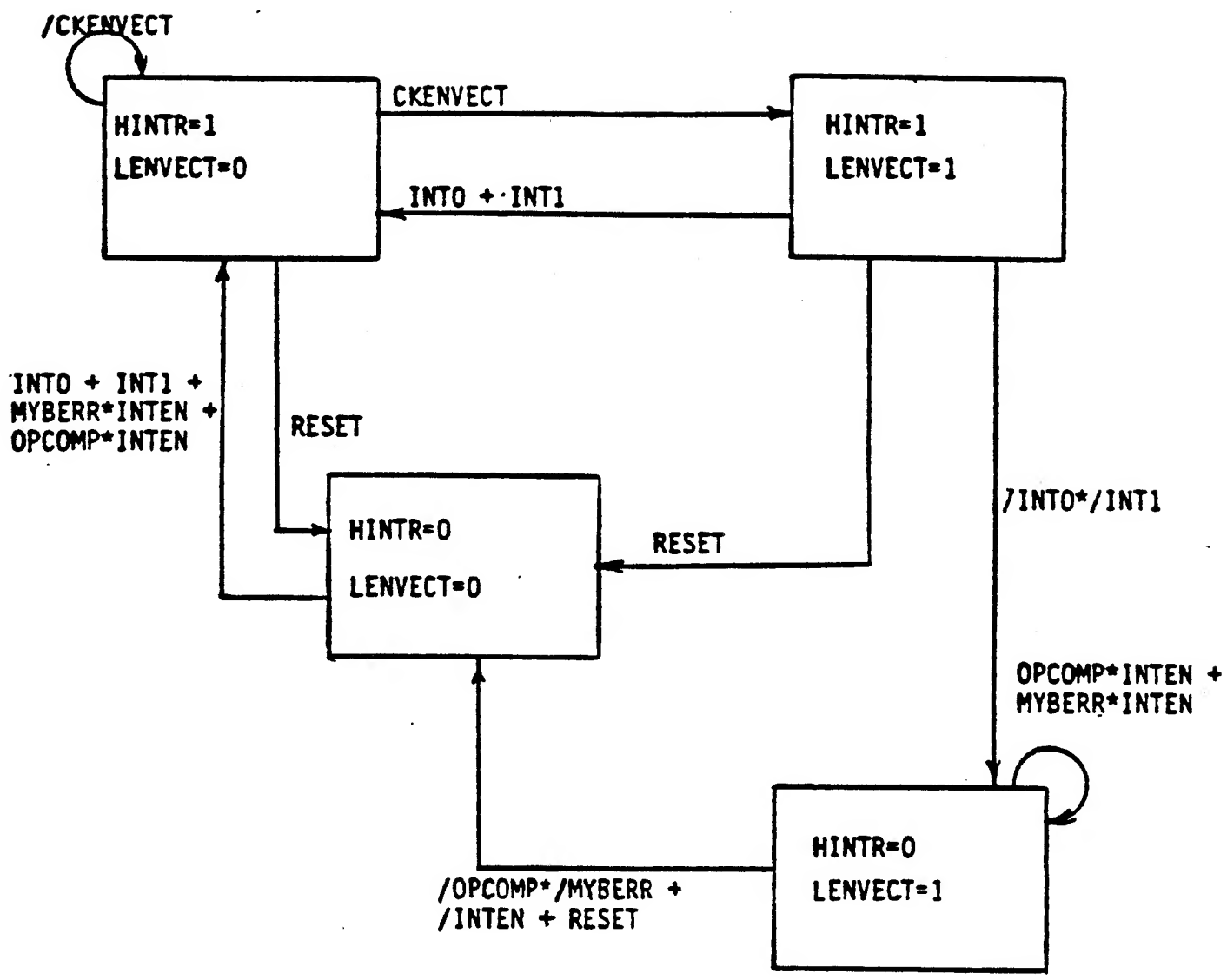
Figure A-7. WDC to BOSS IX System Programmed DMA PAL State Diagram

Table A-2. WDC to BOSS IX System PAL Signal Listing

```
CCLK    /DMAENA   /DRBUS    /FUDR     /PIOOUT    OUT        /PIOINDL   /FLDR   /MSG
/BUSY   DAT       GND       ENB       /REQ       /OPCOMP    /SDATLAT   /LLDR   /ACKOUT
/LDRE   /LUDR     /BRQOUT   /PIOUTF   /HOSTPIO   VCC

ACKOUT     :=  SDATLAT * PIOOUT * REQ * /OUT
            +  ACKOUT * REQ
            =  DMAENA * DAT * REQ * /OUT * SDATLAT * PIOUTF
            +  DMAENA * DAT * REQ * OUT * SDATLAT

BRQOUT     :=  LLDR * DMAENA * DAT * /DRBUS * BUSY
            +  BRQOUT * /DRBUS * DMAENA * BUSY

LUDR       :=  DMAENA * DAT * /OUT * /BRQOUT * /DRBUS
               * PIOUTF * BUSY * /OPCOMP * /LDRE * /HOSTPIO

LLDR       :=  LDRE * PIOUTF * /DRBUS * /OUT * BUSY * /BRQOUT
               * DMAENA * DAT * /OPCOMP /HOSTPIO

PIOUTF      =  REQ * /OUT * SDATLAT * /ACKOUT
            +  PIOUTF * /LUDR * /LLDR * DMAENA * DAT

OPCOMP      =  REQ * /OUT * /DAT * /MSG * /BRQOUT

LDRE       :=  LUDR * /LLDR * BUSY * DMAENA
            +  LDRE * /LLDR * BUSY * DMAENA

SDATLAT    :=  REQ * /OUT * /PIOUTF
            +  SDATLAT * REQ
            +  FUDR * DAT * OUT * DMAENA * BUSY
            +  FLDR * DAT * OUT * DMAENA * BUSY
            +  SDATLAT * /ACKOUT * DMAENA * DAT * OUT * BUSY
            +  FUDR * /BUSY
            +  FLDR * /BUSY
            +  PIOINDL
```

Table A-3. Address PAL and Arbitration PAL Signal Listing

```
PAD1     PAD2     /AB17I   /AB16I   KO       /LDS     /SBUSENA   AS       /WRITE
IBACK    /UDS     GND      /FLDR    /FUDR    /DBDIR   /CKENVECT  /ENVECT  /SCSIOUT
/BDSEL   /ENAUDR  /ENALDR  /SELPIO  /SNBDSEL  VCC

BDSEL    = PAD1 * PAD2 * AS * /AB17I * /AB16I * /KO * /SBUSENA
           * /FUDR * /FLDR
         + PAD1 * PAD2 * AS * /AB17I * /AB16I * /KO * /SBUSENA * SCSIOUT
           * /FUDR * /FLDR
         + PAD1 * PAD2 * AS * /AB17I * /AB16I * KO * /SBUSENA
           * /FUDR * /FLDR
         + PAD1 * PAD2 * AS * /AB17I * /AB16I * KO * /SBUSENA * SCSIOUT
           * /FUDR * /FLDR

ENAUDR   = SNBDSEL * UDS
         + IBACK * /SCSIOUT
         + FUDR * /BDSEL

ENALDR   = SNBDSEL * UDS
         + IBACK * /SCSIOUT
         + FUDR * /BDSEL
         + ENVECT

DBDIR    = SNBDSEL * BDSEL * /WRITE
         + IBACK * /SCSIOUT
         + ENVECT

SLEPIO   = SNBDSEL
         + ENVECT

CKENVEC  = ENVECT * /FUDR * /FLDR * /SBUSENA

BAB3     IACK    BAB1    /BPR2   /BPR1   BAB2    IBRQ    /HINTR   /BGNTI
/HMATCH  SRST    GND     /PFD    DTACK   /REQ1   /CCLK   /BPR0    /RST
IBPR2    IBPR0   IBPR1   /PG1    /RESET  VCC

REQ1     = /BAB1 * BAB2 * /BAB3 * IACK * /DTACK * HINTR
         + IBRQ * BGNTI * /IACK

PG1      = /BPR2 * IBPR1 * HMATCH
         + IBPR2 * HMATCH
         + /BPR1 * IBRP0 * HMATCH
         + /BPR0 * HMATCH

/IBPR2   = /CCLK

/IBPR1   = /CCLK

/IBPR0   = /CCLK

RST      = SRST
         + RESET
         + PFD
```




```
CCLK      INTEN   BERR      INTO     INT1       /CKENVEC   /CLRBER   NC       DRB2
GND       ENB     /OPCOMP   /PIOIN   /PIOINDL   /LENVECT   /MYBERR   /HINTR   /RESET
/ENAUDR   VCC

HINTR    :=  INTO * /RESET
           +  INT1 * /RESET
           +  MYBERR * INTEN * /LENVECT * /RESET
           +  OPCOMP * INTEN * /LENVECT * /RESET

MYBERR   :=  BERR * DRB2 * /RESET
           +  MYBERR * /CLRBER * /RESET

LENVECT  :=  CKENVEC
           +  LENVECT * OPCOMP * INTEN
           +  LENVECT * MYBERR * INTEN

PIOINDL  :=  PIOIN * ENAUDR
```

Figure A-8. Interrupt PAL State Diagram and Signal Listing

Table A-4. Microprocessor Memory and I/O Addressing Map

MEMORY ADDRESS	DESCRIPTION	DATA BITS
0000H TO 3\FFH	8085 FIRMWARE EPROM - 8K	D0-D7
4000H TO 7FFFH	AIC-010 and AIC-300	D0-D7
8000H TO BFFFH	8156 RAM - 256 bytes	D0-D7
C000H TO FFFFH	Not used/Not mapped	

I/O PORT ADDRESS	DESCRIPTION	I/O	DATA BITS
00H TO 7FH	Not Used		
80H	8156 Command Status/Status Register	I/O	D0-D7
81H	8156 I/O Port A	I/O	D0-D7
82H	8156 I/O Port B	Out	D0-D7
83H	8156 I/O Port C	In	D0-D5
84H	8156 Lower Byte of Timer Count	Out	D0-D7
85H	8156 High Byte of Timer Count/Mode	Out	D0-D7
86H to FFH	Not Used		

Table A-5. BOSS IX System I/O Bus (EBUS) Interface Signal Descriptions

SIGNAL	IN/OUT	DESCRIPTIONS
AB00-23	IN/OUT	23-BIT ADDRESS BUS
AS-	IN/OUT	ADDRESS STROBE, TO INDICATE ADDRESS ON THE ADDRESS BUS IS STABLE
BGACK-	IN/OUT	BUS GRANT ACKNOWLEDGE, TO INDICATE BUS CONTROL IS BEING TRANSFERRED
BGNT-	IN	BUS GRANT, TO INDICATE GRANT THE BUS FROM 68000 UP
BERR-	IN	BUS ERROR, TO INDICATE ABNORMAL CONDITION ON THE HOST BUS
BR-	OUT	BUS REQUEST, TO INDICATE ADAPTOR IS REQUESTING USAGE OF BUS
BPR0- to BPR3-	OUT	BUS PRIORITIES, ENCODED PRIORITY ADDRESS USED TO RESOLVE PRIORITIES BY BUS MASTER
CCLK-	IN	CPU CLOCK
DB00-15	IN/OUT	16-BIT DATA BUS, USED TO TRANSFER COMMANDS AND DATA
DTACK-	IN/OUT	DATA TRANSFER ACKNOWLEDGE, ACKNOWLEDGING TRANSFER OF DATA FROM SLAVE
IACK-	IN	INTERRUPT ACKNOWLEDGE, ACKNOWLEDGING AN INTERRUPT REQUEST BY 68000 UP
RESET-	IN	SYSTEM RESET, USED TO RESET ADAPTOR CONTROLLER LOGICS DURING POWER UP OR RESET FROM 68000 UP
R/W-	IN/OUT	READ/WRITE, TO INDICATE DIRECTION OF DATA FLOW BY THE MASTER ON THE BUS
FC2-	IN	FUNCTION CODE, TO INDICATE STATUS OF 68000 UP
LDS-	IN/OUT	LOWER DATA STROBE, TO INDICATE TRANSFER OF THE LOWER 8-BIT DATA BUS
UDS-	IN/OUT	UPPER DATA STROBE, TO INDICATE TRANSFER OF THE UPPER 8-BIT DATA BUS

Table A-6. SCSI Interface Signal Descriptions

SIGNAL	IN/OUT	DESCRIPTIONS
I-/O	IN	IN/OUT, TO INDICATE FLOW DIRECTION OF INFORMATION ON THE SCSI BUS
C-/D	IN	COMMAND/DATA, TO INDICATE WHETHER INFORMATION ON THE BUS IS COMMAND OR DATA
BUSY-	IN	BUSY, TO INFORM ADAPTOR THAT CONTROLLER IS READY TO CONDUCT TRANSACTIONS
MSG-	IN	MESSAGE, TO INDICATE THAT SCSI BUS IS IN THE MESSAGE PHASE
REQ-	IN	REQUEST, TO REQUEST A BYTE FROM ADAPTOR OR TO INDICATE THAT DATA ON BUS IS STABLE
ACK-	OUT	ACKNOWLEDGE, TO INDICATE TO CONTROLLER THAT ADAPTOR HAS ALREADY TAKEN A BYTE OR THAT DATA ON THE BUS IS STABLE
RST-	OUT	RESET, TO FORCE THE CONTROLLER INTO AN IDLE STATE
SEL-	OUT	SELECT, TO INITIATE A COMMAND TRANSACTION
SD7- to SD0-	IN/OUT	8-BIT DATA BUS, USED TO TRANSFER COMMANDS AND DATA

Table A-7. Drive Interface Signal Descriptions

SIGNAL	IN/OUT	DESCRIPTIONS
RWC-	OUT	REDUCED WRITE CURRENT, SIGNAL TO WRITE ON DISK WITH A LOWER WRITE CURRENT
WGATE-	OUT	WRITE GATE, SIGNAL ENABLES WRITE DATA TO BE WRITTEN ON THE DISK
SKCOMP-	IN	SEEK COMPLETE, SIGNAL TRUE WHEN R/W HEADS HAVE SETTLED ON FINAL TRACK
TRK0-	IN	TRACK ZERO, SIGNAL TRUE WHEN R/W HEADS HAVE SETTLED ON TRACK ZERO
WFLT-	IN	WRITE FAULT, INDICATES CONDITION EXISTS WHICH CAUSES IMPROPER WRITING
INDEX-	IN	INDEX, SIGNAL INDICATES THE BEGINNING OF A TRACK
DRDY-	IN	DRIVE READY, INDICATES THAT DRIVE READY TO READ, WRITE, SEEK, AND VALID I/O SIGNALS
STEP-	OUT	STEP, CONTROL LINE WHICH CAUSES R/W HEADS TO MOVE
DRSELX	OUT	DRIVE SELECT, SIGNALS CONNECT DRIVES TO INTERFACE LOGIC
HDSELX	OUT	HEAD SELECT, SIGNALS TO SELECT HEADS IN A BINARY CODED SEQUENCE
DIRIN-	OUT	DIRECTION IN, DEFINES DIRECTION OF HEAD MOVEMENT
WDATXX	OUT	MFM DIFFERENTIAL WRITE DATA

Table A-8. List of WDC Mnemonics

SIGNAL NAMES	DESCRIPTION
AB01-23	BOSS IX SYSTEM ADDRESS BUS BITS 01 THROUGH 23
ACKIN	ACKNOWLEDGE DATA IN TO CONTROLLER SECTION
ACKOUT	ACKNOWLEDGE DATA OUT FROM CONTROLLER SECTION
BACK	HOST ACKNOWLEDGE BUS REQUEST
BD0-8	BUFFERED DATA BITS 0 THROUGH 8
BDSEL	HOST ACCESS/SELECT WDC BOARD
BERR	BOSS IX SYSTEM BUS ERROR
BGNT	BOSS IX SYSTEM BUS GRANT
CCLK	HOST CPU CLOCK
CLRBER	CLEAR BUS ERROR LATCH
DB00-15	BOSS IX SYSTEM DATA BUS BIT 00 THROUGH 15
DBDIR	DATA BUS DIRECTION
DMADRL	LOAD LOWER DMA ADDRESS REGISTER
DMADRM	LOAD MIDDLE DMA ADDRESS REGISTER
DMADRH	LOAD HIGHER DMA ADDRESS REGISTER
DRBUS	DRIVE BOSS IX SYSTEM BUS
DTACK	BOSS IX SYSTEM DATA TRANSFER ACKNOWLEDGE
ENALDR	ENABLE LOWER DATA TRANSCEIVER

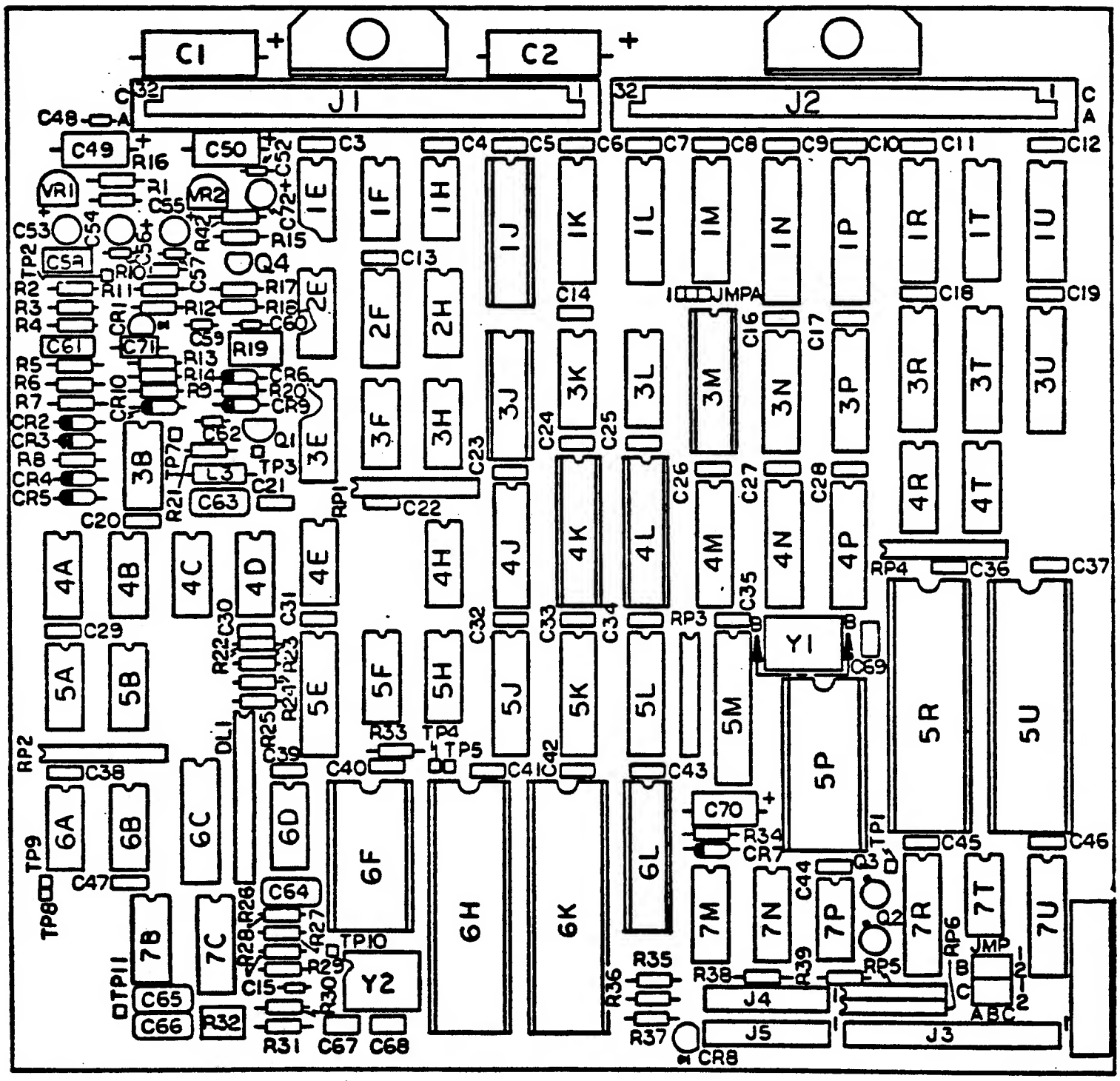


Figure A-9. Part No. 903496, Parts Location Diagram

Table A-9. Part No. 903496-001, List of Parts (Sheet 1 of 3)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0001	905019-001	PCBA 5 1/4 WDC CONTROLLER	*
0003	762022-003	LABEL TAB .375X1.250 YEL	*
0005	101514	IC 7438 BUFFER QUAD 2 INPUT NAND	6D
0010	168014-001	IC 74S132 QUAD 2-INPUT NAND, SCHMITT TRIG	4A
0011	168000-006	IC 74F64 4-2-3-2 AND OR INV GATE	5A
0012	168000-008	IC 74F74 DUAL D-TYPE FLIP/FLOP	4D
0014	101710	IC 74LS02 QUAD 2 IN NOR	5H
0016	101781	IC 74LS27 TRIPLE 3-IN NOR GATE	7T
0017	101714	IC 74LS32 QUAD 2-IN OR	7P
0018	101741	IC 74LS74 DUAL D-TYPE POS EDG-TRIG F/F	4E,7B
0019	161062-001	IC 74LS123 DUAL ONE SHOT	7C
0020	101719	IC 74LS138 3-8 LINE DECODER/DEMPLEX.	3L
0021	161064-001	IC 74LS240 BUFF LINE DR 3-ST OCTAL	4J,4M,5J,5L, 6C,7R
0022	161068-001	IC 74LS244 OCTAL BUFFER/LINE DRIVER	3P
0023	161023	IC 74LS273 OCTAL D-TYPE FLIP/FLOP	3N
0024	161013	IC 74LS373 OCTAL D-TYPE LATCH 3-STATE	4P
0025	161065-001	IC 74LS374 OCTAL REGISTER D-TYPE F/F	4N
0026	168002-007	IC 74F533 OCTL TRNSPRNT LATCH (3STATE)	5K
0027	168012-001	IC 74LS648 OCTAL BUS TRNSRCVR/REGISTER	1N,1P,5M
0028	161151-001	IC 74LS699 SYNC U/D COUNT/REG	1R,1T,1U,3R, 3T,3U
0035	101315	IC 74S00 QUAD 2 INPUT POS NAND GATE	3B,3H
0036	101655	IC 74S02 POS-NOR GATE TOTEM-POLE	2H,5F
0037	101615	IC 74S08 QUAD 2 INPUT POS AND GATE	4T
0038	101623	IC-74S11 3 INPUT AND	4H
0039	101625	IC 74S32 QUAD 2 INPUT POSITIVE-OR GATE	3F
0040	101627	IC SN74S38 QUAD 2 INPUT POS NAND BUFF	1F,1H
0041	101629	IC SN74S74 DUAL D-TYPE FLIP/FLOP	1E,2E,4B,4C, 5B,6A,6B
0042	101630	IC 74S112 DUAL J-K EDGE TRIG FLIP/FLOP	2F,3E
0043	161009	IC 74S240 OCTAL BUFFER 3STATE TTL	1K,1L,5E,7U
0044	161074-001	IC 74S244 OCTAL BUFFER	1M
0045	101637	IC SN74S260 DUAL 5 INPUT POS-NOR GATE	4R
0046	101631	IC 74S138 DECODER/DEMULTIPLEXER	3K
0050	911017-001	IC PAL FAST 20L8A-WDC BUS ARBITRATION	1J
0051	911017-004	IC PAL FAST 20L8A WDC ADDRESS DECODER	3M
0052	911018-001	IC PAL FAST 20R6A-WDC HOST/CONT SEQ	4K
0053	911018-002	IC PAL FAST 20R6A-WDC CONT/HOST SEQ	4L
0054	911003-008	IC PAL HIGH SPEED 16RA-INTERRUPT CTL	3J
0060	162062-001	IC STATIC RAM 2KX8 S/LINE 150NS	6L
0061	400569-003	PROC SPEC IC DUAL PORT BFR CNT AIC-300	6K
0062	400569-001	PROC SPEC SER/DESERIALIZER AIC-010	6H
0063	400569-002	PROC SPEC IC ENCODE/DECODE AIC-250	6F
0064	161157-001	IC QUAD DIFFRNTL LINE RECIEVER 3486	7M
0065	161158-001	IC QUAD DIFFRNTL LINE DRIVER 3487	7N
0066	162059-001	IC 8-BIT NMOS MICROPROCESOR (8085A)	5R
0067	165053-002	IC PROM 8K X 8 2764 300NS WDC FRMWRE	5P

Table A-9. Part No. 903496-001, List of Parts (Sheet 2 of 3)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0068	162058-001	IC 2048-BIT STATIC RAM W/ I/O PRT-TMR	5U
0070	111000-095	RES CARBON FILM .25W 5% 51 OHM	R1
0071	111000-043	RES CARBON FILM .25W 5% 100 OHM	R14,20,26, 33,36,37
0073	111000-048	RES CARBON FILM .25W 5% 220 OHM	R22,24,27
0074	111000-029	RES CARBON FILM .25W 5% 330 OHM	R4,5,23,25, 35
0075	111000-051	RES CARBON FILM .25W 5% 390 OHM	R21
0076	111000-055	RES CARBON FILM .25W 5% 680 OHM	R3
0077	111000-031	RES CARBON FILM .25W 5% 1K OHM	R39
0078	111000-060	RES CARBON FILM .25W 5% 4.7KOHM	R31
0079	111000-063	RES CARBON FILM .25W 5% 10K OHM	R2,38
0080	111000-004	RES CARBON FILM .25W 5% 75K OHM	R34
0081	111000-071	RES CARBON FILM .25W 5% 100K OHM	R13
0082	111000-072	RES CARBON FILM .25W 5% 1.0K OHM	R12
0083	111000-054	RES CARBON FILM .25W 5% 620 OHM	R9
0090	116000-003	RES METAL FILM .125W 1% 511 OHM	R29
0091	116000-175	RES METAL FILM .125W 1% 1.10K OHM	R8
0092	116000-241	RES METAL FILM .125W 1% 1.02K OHM	R28
0093	116000-156	RES METAL FILM .125W 1% 1.65K OHM	R7
0094	116000-158	RES METAL FILM .125W 1% 1.96K OHM	R17,18
0095	116000-183	RES METAL FILM .125W 1% 2.67K OHM	R6
0096	116000-161	RES METAL FILM .125W 1% 3.09K OHM	R10,11,30
0097	111000-045	RES CARBON FILM .25W 5% 150 OHM	R42
0098	111000-124	RES CARBON FILM .25W 5% 430 OHM	R15
0099	111000-052	RES CARBON FILM .25W 5% 470 OHM	R16
0100	118004-005	POT SQ CERMET .5W MULTI TURN 2.0K OHM	R19
0101	118004-009	POT SQ CERMET .5W MULTI TURN 50K OHM	R32
0105	101054	RES NTWK 8 PIN SIP 220 OHM	RP6
0106	119004-004	RES NTWK SIP LP 10PIN 9 RES 1.0K OHM	RP3
0107	101055	RES NTWK 8 PIN SIP 330 OHM	RP5
0108	119017-004	RES NTWK SIP C/C 10 PIN 9 RES 2.2K OHM	RP1,2,4
0109	151004-001	CRYSTAL PARALLEL RESONANCE 6.0MHZ 30PF	Y1
0110	101336	CRYSTAL FUND 10.000MHZ .005%	Y2
0111	155003-001	IC DELAY LINE 10 TAPS 100 OHMS -100NS	DL1
0115	152001-001	DIODE LIGHT EMITTING GREEN DIFF LENS	CR8
0116	130006-001	DIODE SWITCHING 1N914B	CR2,3,4,5,6, 7,9,10
0117	130028-001	DIODE VAPACTOR HIGH CAP 400-500PF	CR1
0123	103000-010	CAP MICA DIPPED RADIAL 51PF 5% 500V	C64
0124	103000-009	CAP MICA DIPPED RADIAL 10PF 5% 500V	C65,66
0125	103000-007	CAP MICA DIPPED RADIAL 18PF 5% 300V	C67,68,69
0126	103000-008	CAP MICA DIPPED RADIAL 150PF 5% 500V	C61
0127	103000-018	CAP MICA DIPPED RADIAL 330PF 5% 100V	C58
0128	103000-012	CAP MICA DIPPED RADIAL 270PF 1% 500V	C63
0130	104012-012	CAP CERAMIC COG AXIAL 6800PF 5% 50V	C71
0131	104010-001	CAP CERAMIC Z5U AXL .1UF +80 -20% 50V	C3-48,52,56, 57,59,60,62
0132	102004-014	CAP SOLID TANTALUM RDAL 4.7UF 20% 35V	C53,54,55,72

Table A-9. Part No. 903496-001, List of Parts (Sheet 3 of 3)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0133	102000-001	CAP SOLID TANTALUM AXIAL 15UF 10% 20V	C49,50,70
0134	108016-004	CAP ALUM ELECT 100 UF +75 -20% 6V	C1,2
0140	140005-001	TRANS NPN GEN PURP 2N3904 CASE TO-92	Q1
0141	140028-001	TRANSISTOR NPN LOW VOLT SILICON SW	Q2,3
0142	141022-001	TRANS PNP 2N5771	Q4
0145	135041-001	INDUCTOR,2.2UH SHIELDED 10%	L3
0150	132016-001	IC 78L05 3TERM FIX +5.0V POS VOLT REG	VR2
0151	132015-001	IC 79L05 3TERM FIX -5.0V NEG VOLT REG	VR1
0160	300092-001	CONN DIN FML 3X32 PRESS-FIT 64 POS A&C	J1,J2
0161	310019-001	CONN HOUSING/GUIDE DIN 3X32 .100CTS ML	(J1,J2)
0162	907388-001	EJECTOR EURO-DIN CONN STACK	*
0163	907769-001	LATCH EURO-DIN CONNECTOR STACK	*
0164	907985-001	CATCH PCBA STACK CONTROLLERS	*
0165	214027-001	FASTENER PUSH-ON .312 DIA STUD	*
0170	300032-016	CONN HDR DBL ROW .100CTS .025SQ 34POS	J3
0171	300032-009	CONN HDR DBL ROW .100CTS .025SQ 20POS	J4,J5
0174	325005-011	SOCKET IC DIP 4-LEAF CONT GOLD 20POS	(3J)
0175	325005-012	SOCKET IC DIP 4-LEAF GOLD 24POS .300	(1J,3M,4K, 4L)
0176	325005-007	SOCKET IC DIP 4-LEAF CONT GOLD 28POS	(5P)
0177	325005-010	SOCKET IC DIP 4-LEAF CONT GOLD 40POS	(5R,5U,6H, 6K)
0178	325005-001	SOCKET IC DIP 4-LEAF CONT GOLD 24POS	(6F)
0179	700023	TAPE DOUBLE SIDED .50 WIDE	(Y1,Y2)
0180	300032-002	CONN HDR DBL ROW .100CTS .025SQ 6POS	JUMP B,C
0181	325026-003	CONN HDR SGL ROW .100CTS .025SQ 3POS	JUMP A
0182	325033-001	JUMPER 0.025 SQ 0.100 CENTERS GOLD PL	(JUMP A, B & C)

Table A-10. Part No. 903496-002, List of Parts (Sheet 1 of 3)

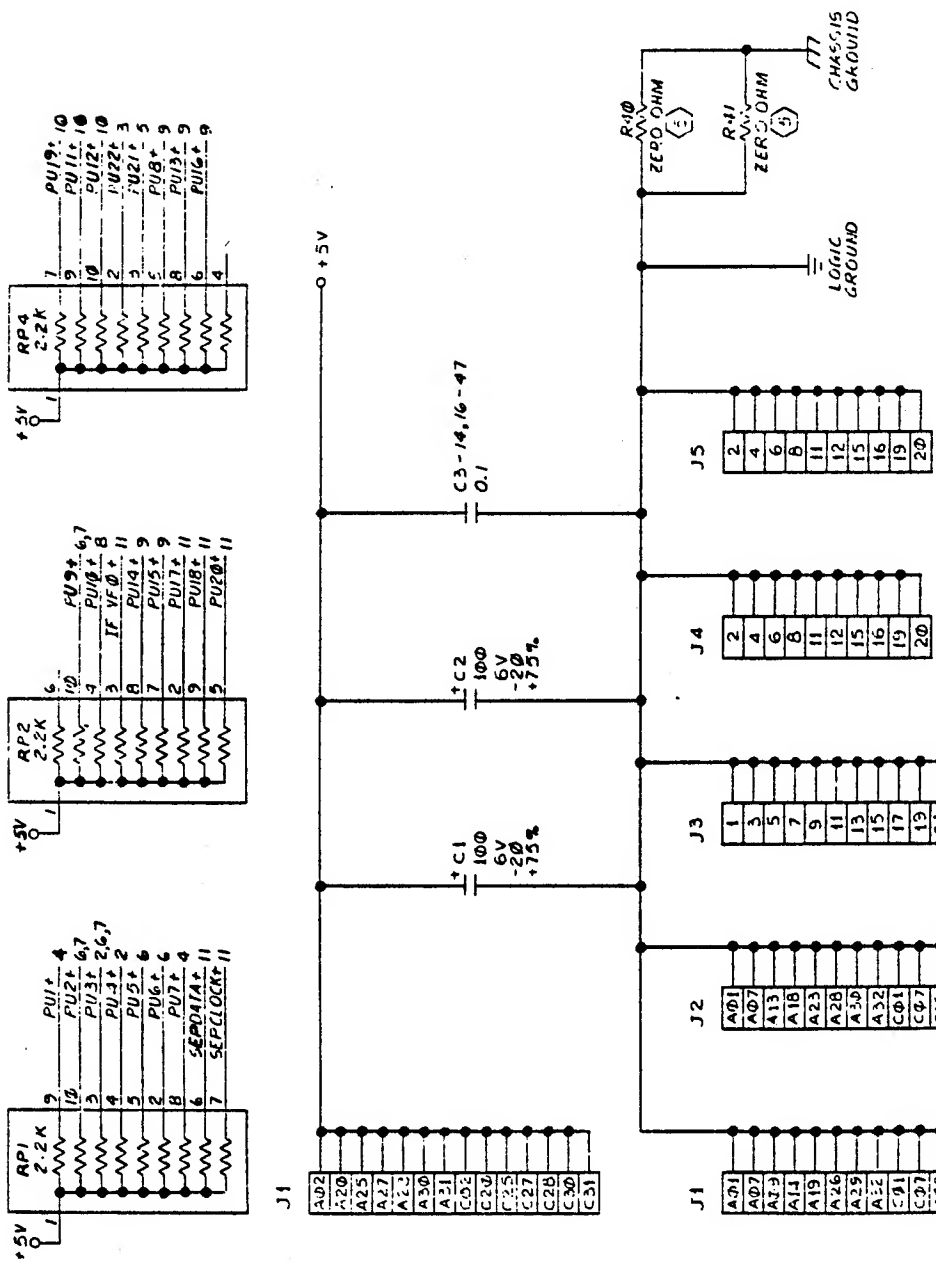
REF NO.	PART NO.	DESCRIPTION	REFERENCE
0001	905019-001	PCBA 5 1/4 WDC CONTROLLER	*
0003	762022-003	LABEL TAB .375X1.250 YEL	*
0005	101514	IC 7438 BUFFER QUAD 2 INPUT NAND	6D
0010	168014-001	IC 74S132 QUAD 2-INPUT NAND, SCHMITT TRIG	4A
0011	168000-006	IC 74F64 4-2-3-2 AND OR INV GATE	5A
0012	168000-008	IC 74F74 DUAL D-TYPE FLIP/FLOP	4D
0014	101710	IC 74LS02 QUAD 2 IN NOR	5H
0016	101781	IC 74LS27 TRIPLE 3-IN NOR GATE	7T
0017	101714	IC 74LS32 QUAD 2-IN OR	7P
0018	101741	IC 74LS74 DUAL D-TYPE POS EDG-TRIG F/F	4E,7B
0019	161062-001	IC 74LS123 DUAL ONE SHOT	7C
0020	101719	IC 74LS138 3-8 LINE DECODER/DEMPLEX.	3L
0021	161064-001	IC 74LS240 BUFF LINE DR 3-ST OCTAL	4J,4M,5J,5L, 6C,7R
0022	161068-001	IC 74LS244 OCTAL BUFFER/LINE DRIVER	3P
0023	161023	IC 74LS273 OCTAL D-TYPE FLIP/FLOP	3N
0024	161013	IC 74LS373 OCTAL D-TYPE LATCH 3-STATE	4P
0025	161065-001	IC 74LS374 OCTAL REGISTER D-TYPE F/F	4N
0026	168002-007	IC 74F533 OCTL TRNSPRNT LATCH (3STATE)	5K
0027	168012-001	IC 74LS648 OCTAL BUS TRNSRCVR/REGISTER	1N,1P,5M
0028	161151-001	IC 74LS699 SYNC U/D COUNT/REG	1R,1T,1U,3R, 3T,3U
0035	101315	IC 74S00 QUAD 2 INPUT POS NAND GATE	3B,3H
0036	101655	IC 74S02 POS-NOR GATE TOTEM-POLE	2H,5F
0037	101615	IC 74S08 QUAD 2 INPUT POS AND GATE	4T
0038	101623	IC-74S11 3 INPUT AND	4H
0039	101625	IC 74S32 QUAD 2 INPUT POSITIVE-OR GATE	3F
0040	101627	IC SN74S38 QUAD 2 INPUT POS NAND BUFF	1F,1H
0041	101629	IC SN74S74 DUAL D-TYPE FLIP/FLOP	1E,2E,4B,4C, 5B,6A,6B
0042	101630	IC 74S112 DUAL J-K EDGE TRIG FLIP/FLOP	2F,3E
0043	161009	IC 74S240 OCTAL BUFFER 3STATE TTL	1K,1L,5E,7U
0044	161074-001	IC 74S244 OCTAL BUFFER	1M
0045	101637	IC SN74S260 DUAL 5 INPUT POS-NOR GATE	4R
0046	101631	IC 74S138 DECODER/DEMULTIPLEXER	3K
0050	911017-007	IC PAL FAST 20L8A-2ND WDC BUS ARBTRTN	1J
0051	911017-004	IC PAL FAST 20L8A WDC ADDRESS DECODER	3M
0052	911018-001	IC PAL FAST 20R6A-WDC HOST/CONT SEQ	4K
0053	911018-002	IC PAL FAST 20R6A-WDC CONT/HOST SEQ	4L
0054	911003-008	IC PAL HIGH SPEED 16RA-INTERRUPT CTL	3J
0060	162062-001	IC STATIC RAM 2KX8 S/LINE 150NS	6L
0061	400569-003	PROC SPEC IC DUAL PORT BFR CNT AIC-300	6K
0062	400569-001	PROC SPEC SER/DESERIALIZER AIC-010	6H
0063	400569-002	PROC SPEC IC ENCODE/DECODE AIC-250	6F
0064	161157-001	IC QUAD DIFFRNTL LINE RECIEVER 3486	7M
0065	161158-001	IC QUAD DIFFRNTL LINE DRIVER 3487	7N
0066	162059-001	IC 8-BIT NMOS MICROPROCESOR (8085A)	5R
0067	165053-005	IC PROM 8K X 8 2764 300NS WDC FRMWRE	5P

Table A-10. Part No. 903496-002, List of Parts (Sheet 2 of 3)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0068	162058-001	IC 2048-BIT STATIC RAM W/ I/O PRT-TMR	5U
0070	111000-095	RES CARBON FILM .25W 5% 51 OHM	R1
0071	111000-043	RES CARBON FILM .25W 5% 100 OHM	R14,20,26, 33,36,37
0073	111000-048	RES CARBON FILM .25W 5% 220 OHM	R22,24,27
0074	111000-029	RES CARBON FILM .25W 5% 330 OHM	R4,5,23,25, 35
0075	111000-051	RES CARBON FILM .25W 5% 390 OHM	R21
0076	111000-055	RES CARBON FILM .25W 5% 680 OHM	R3
0077	111000-031	RES CARBON FILM .25W 5% 1K OHM	R39
0078	111000-060	RES CARBON FILM .25W 5% 4.7KOHM	R31
0079	111000-063	RES CARBON FILM .25W 5% 10K OHM	R2,38
0080	111000-004	RES CARBON FILM .25W 5% 75K OHM	R34
0081	111000-071	RES CARBON FILM .25W 5% 100K OHM	R13
0082	111000-072	RES CARBON FILM .25W 5% 1.0K OHM	R12
0083	111000-054	RES CARBON FILM .25W 5% 620 OHM	R9
0090	116000-003	RES METAL FILM .125W 1% 511 OHM	R29
0091	116000-175	RES METAL FILM .125W 1% 1.10K OHM	R8
0092	116000-241	RES METAL FILM .125W 1% 1.02K OHM	R28
0093	116000-156	RES METAL FILM .125W 1% 1.65K OHM	R7
0094	116000-158	RES METAL FILM .125W 1% 1.96K OHM	R17,18
0095	116000-183	RES METAL FILM .125W 1% 2.67K OHM	R6
0096	116000-161	RES METAL FILM .125W 1% 3.09K OHM	R10,11,30
0097	111000-045	RES CARBON FILM .25W 5% 150 OHM	R42
0098	111000-124	RES CARBON FILM .25W 5% 430 OHM	R15
0099	111000-052	RES CARBON FILM .25W 5% 470 OHM	R16
0100	118004-005	POT SQ CERMET .5W MULTI TURN 2.0K OHM	R19
0101	118004-009	POT SQ CERMET .5W MULTI TURN 50K OHM	R32
0105	101054	RES NTWK 8 PIN SIP 220 OHM	RP6
0106	119004-004	RES NTWK SIP LP 10PIN 9 RES 1.0K OHM	RP3
0107	101055	RES NTWK 8 PIN SIP 330 OHM	RP5
0108	119017-004	RES NTWK SIP C/C 10 PIN 9 RES 2.2K OHM	RP1,2,4
0109	151004-001	CRYSTAL PARALLEL RESONANCE 6.0MHZ 30PF	Y1
0110	101336	CRYSTAL FUND 10.000MHZ .005%	Y2
0111	155003-001	IC DELAY LINE 10 TAPS 100 OHMS -100NS	DL1
0115	152001-001	DIODE LIGHT EMITTING GREEN DIFF LENS	CR8
0116	130006-001	DIODE SWITCHING 1N914B	CR2,3,4,5,6, 7,9,10
0117	130028-001	DIODE VAPACTOR HIGH CAP 400-500PF	CR1
0123	103000-010	CAP MICA DIPPED RADIAL 51PF 5% 500V	C64
0124	103000-009	CAP MICA DIPPED RADIAL 10PF 5% 500V	C65,66
0125	103000-007	CAP MICA DIPPED RADIAL 18PF 5% 300V	C67,68,69
0126	103000-008	CAP MICA DIPPED RADIAL 150PF 5% 500V	C61
0127	103000-018	CAP MICA DIPPED RADIAL 330PF 5% 100V	C58
0128	103000-012	CAP MICA DIPPED RADIAL 270PF 1% 500V	C63
0130	104012-012	CAP CERAMIC COG AXIAL 6800PF 5% 50V	C71
0131	104010-001	CAP CERAMIC Z5U AXL .1UF +80 -20% 50V	C3-48,52,56, 57,59,60,62
0132	102004-014	CAP SOLID TANTALUM RDAL 4.7UF 20% 35V	C53,54,55,72

Table A-10. Part No. 903496-002, List of Parts (Sheet 3 of 3)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0133	102000-001	CAP SOLID TANTALUM AXIAL 15UF 10% 20V	C49,50,70
0134	108016-004	CAP ALUM ELECT 100 UF +75 -20% 6V	C1,2
0140	140005-001	TRANS NPN GEN PURP 2N3904 CASE TO-92	Q1
0141	140028-001	TRANSISTOR NPN LOW VOLT SILICON SW	Q2,3
0142	141022-001	TRANS PNP 2N5771	Q4
0145	135041-001	INDUCTOR,2.2UH SHIELDED 10%	L3
0150	132016-001	IC 78L05 3TERM FIX +5.0V POS VOLT REG	VR2
0151	132015-001	IC 79L05 3TERM FIX -5.0V NEG VOLT REG	VR1
0160	300092-001	CONN DIN FML 3X32 PRESS-FIT 64 POS A&C	J1,J2
0161	310019-001	CONN HOUSING/GUIDE DIN 3X32 .100CTS ML	(J1,J2)
0162	907388-001	EJECTOR EURO-DIN CONN STACK	*
0163	907769-001	LATCH EURO-DIN CONNECTOR STACK	*
0164	907985-001	CATCH PCBA STACK CONTROLLERS	*
0165	214027-001	FASTENER PUSH-ON .312 DIA STUD	*
0170	300032-016	CONN HDR DBL ROW .100CTS .025SQ 34POS	J3
0171	300032-009	CONN HDR DBL ROW .100CTS .025SQ 20POS	J4,J5
0174	325005-011	SOCKET IC DIP 4-LEAF CONT GOLD 20POS	(3J)
0175	325005-012	SOCKET IC DIP 4-LEAF GOLD 24POS .300	(1J,3M,4K, 4L)
0176	325005-007	SOCKET IC DIP 4-LEAF CONT GOLD 28POS	(5P)
0177	325005-010	SOCKET IC DIP 4-LEAF CONT GOLD 40POS	(5R,5U,6H, 6K)
0178	325005-001	SOCKET IC DIP 4-LEAF CONT GOLD 24POS	(6F)
0179	700023	TAPE DOUBLE SIDED .50 WIDE	(Y1,Y2)
0180	300032-002	CONN HDR DBL ROW .100CTS .025SQ 6POS	JUMP B,C
0181	325026-003	CONN HDR SGL ROW .100CTS .025SQ 3POS	JUMP A
0182	325033-001	JUMPER 0.025 SQ 0.100 CENTERS GOLD PL	(JUMP A, B & C)



REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R42	—
RP6	—
C72	C51
Y2	—
CR10	—
Q4	—
L3	L1,2
VR2	—
J5	—
TP11	TP6
DL1	—
JMPC	—

POWER CHART (UNLESS OTHERWISE SPECIFIED)					
DEVICE	+5V&5VØ Ø	GND	+12V	-12V	-5V
14	14	7	—	—	—
16	16	8	—	—	—
2Ø	2Ø	1Ø	—	—	—
24LOSCMTR	24	12	—	—	—
24LOGCMTR	24	1Ø	—	—	—
28	28	14	—	—	—
4Ø	4Ø	2Ø	—	—	—

SPARE CHART			
LOCATION	IC TYPE	QTY	PIN NOS OF SPARES
4A	74S132	2	1,2,3,8,9,1Ø
5H	74LS1Ø2	2	1,2,3,4,5,6
5J	74LS24Ø	1	3,11
5F	74S1Ø2	3	1,2,3,8,9,1Ø,11,12,13
6C	74LS24Ø	1	1,13
7B	74LS74	1	8,9,1Ø,11,12,13
7M	3486	2	5,6,7,9,1Ø,11
7N	3487	2	5,6,7,9,1Ø,11
7R	74LS24Ø	2	4,6,14,16
7T	74LS27	1	8,9,1Ø,11
RP2	2.2K PU	1	6
RP3	1.ØK PU	1	2
RP4	2.2K PU	1	4
RP5	33Ø Ω PD	2	2,3
RP6	22Ø Ω PU	2	2,3

BOARD ADDRESS JMP A		
ASSEMBLY P/N	JUMPER	BOARD ADDRESS
903496-001	1-2	CCXXXX HEX
903496-002	2-3	COXXXX HEX

WRITE PRECOMPENSATION	
JUMPER B JUMPER C	DRIVE Ø DRIVE 1
JMP B OR C	WRITE PRECOMP
1A - 2A	ALWAYS OFF
1B - 2B	ALWAYS ON
1C - 2C	SAME CYLINDER AS REDUCED WRITE CURRENT

Figure A-10. Part No. 903496, Schematic Diagram (Sheet 1 of 12)

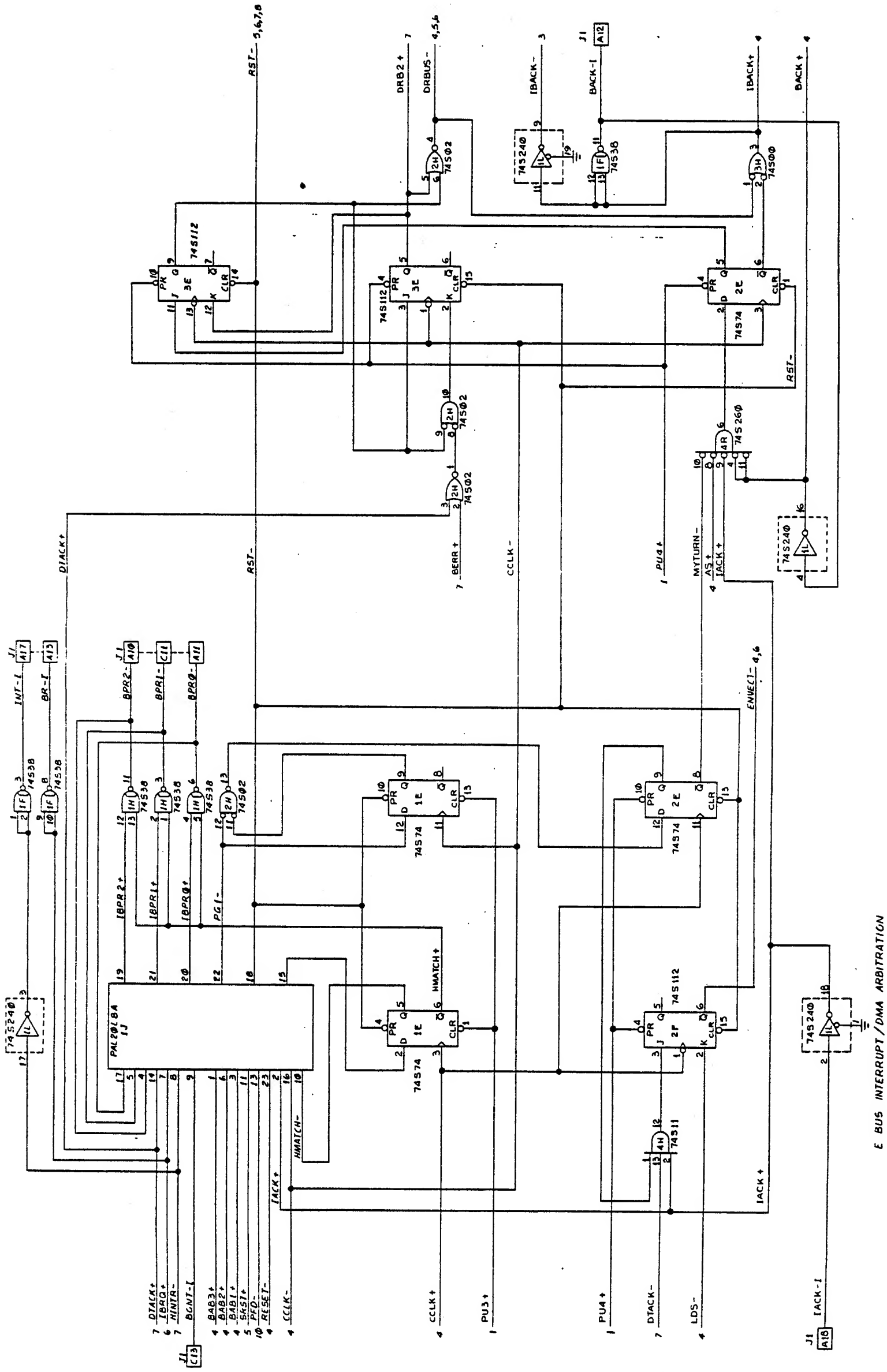


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 2 of 12)

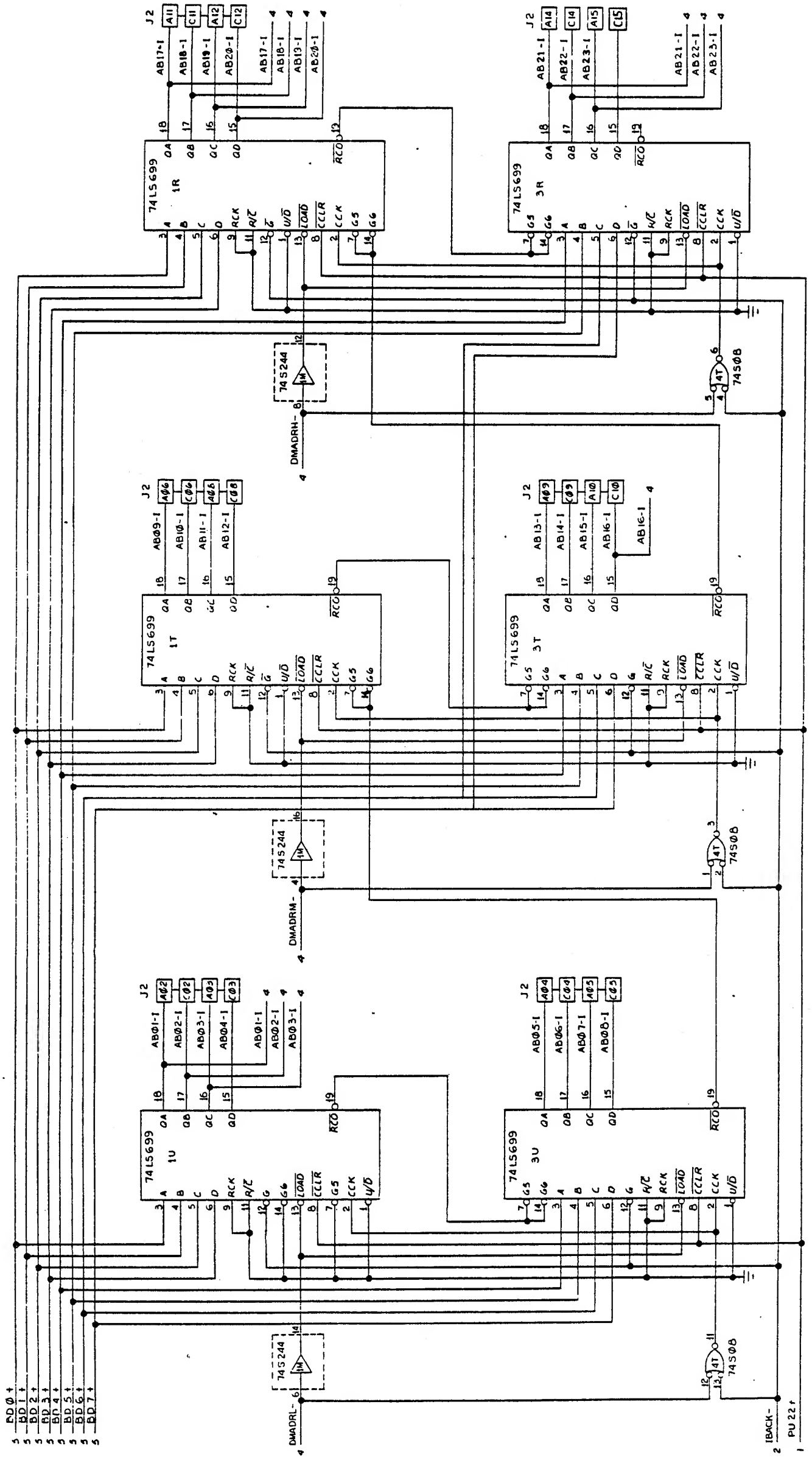


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 3 of 12)

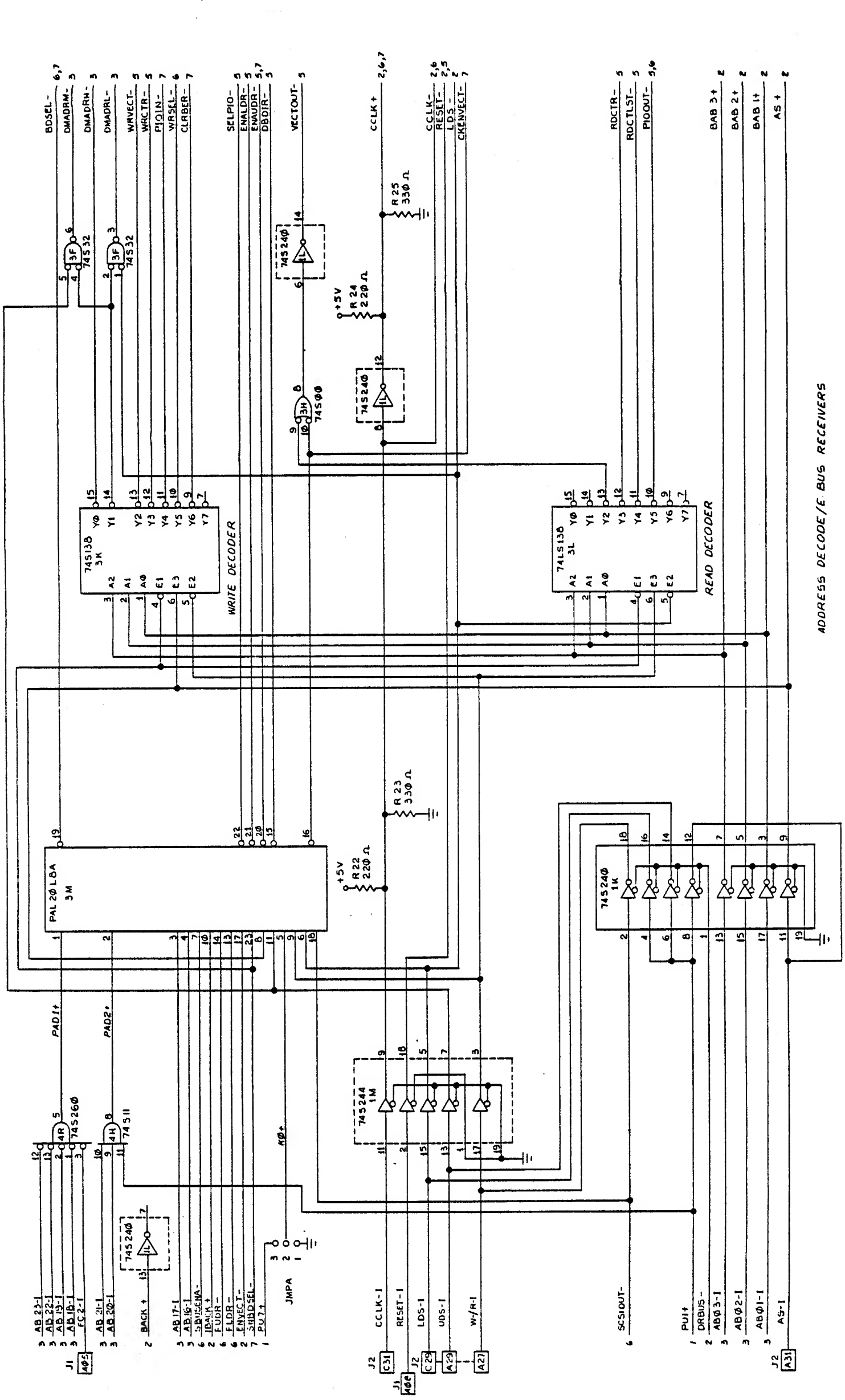


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 4 of 12)

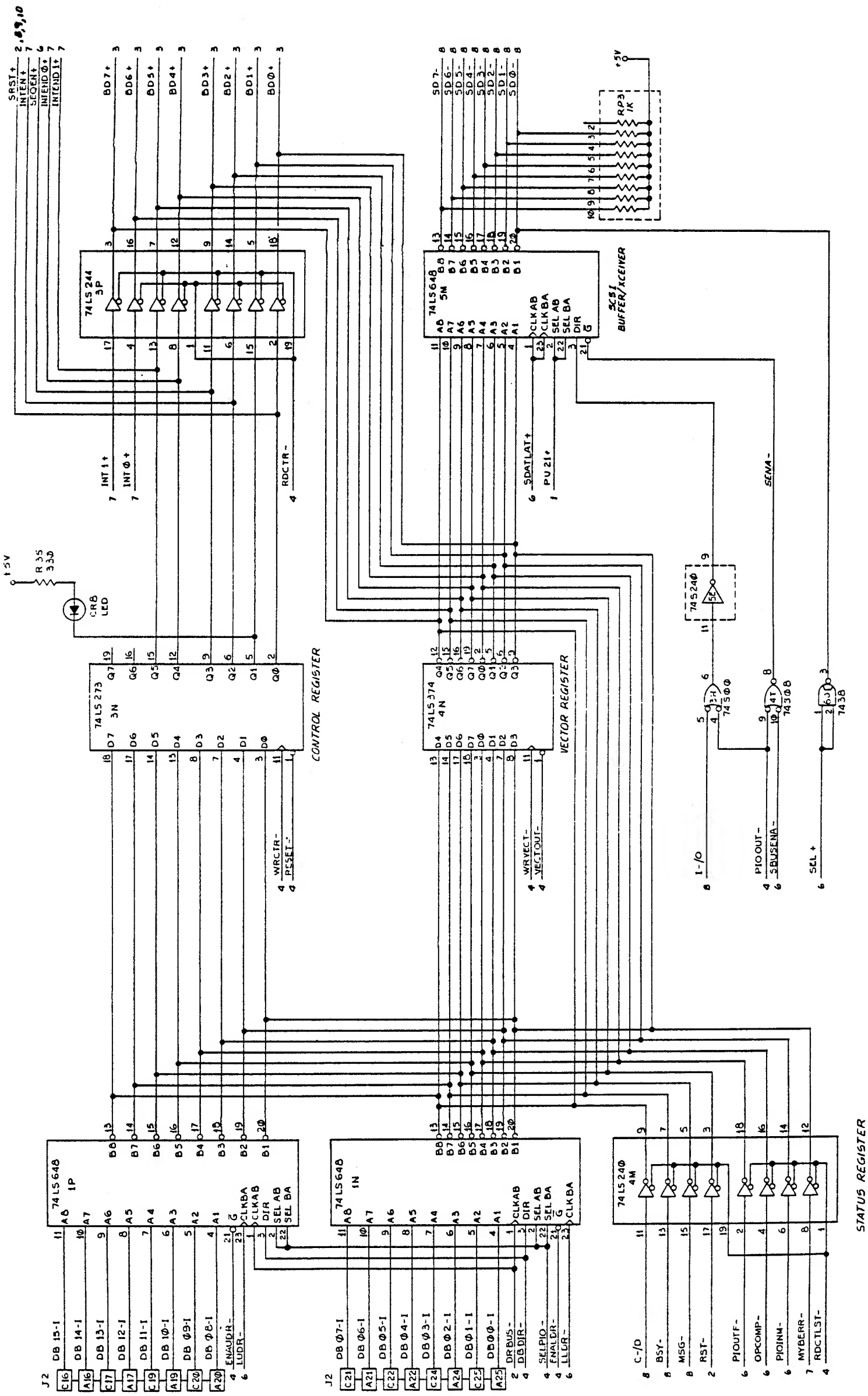
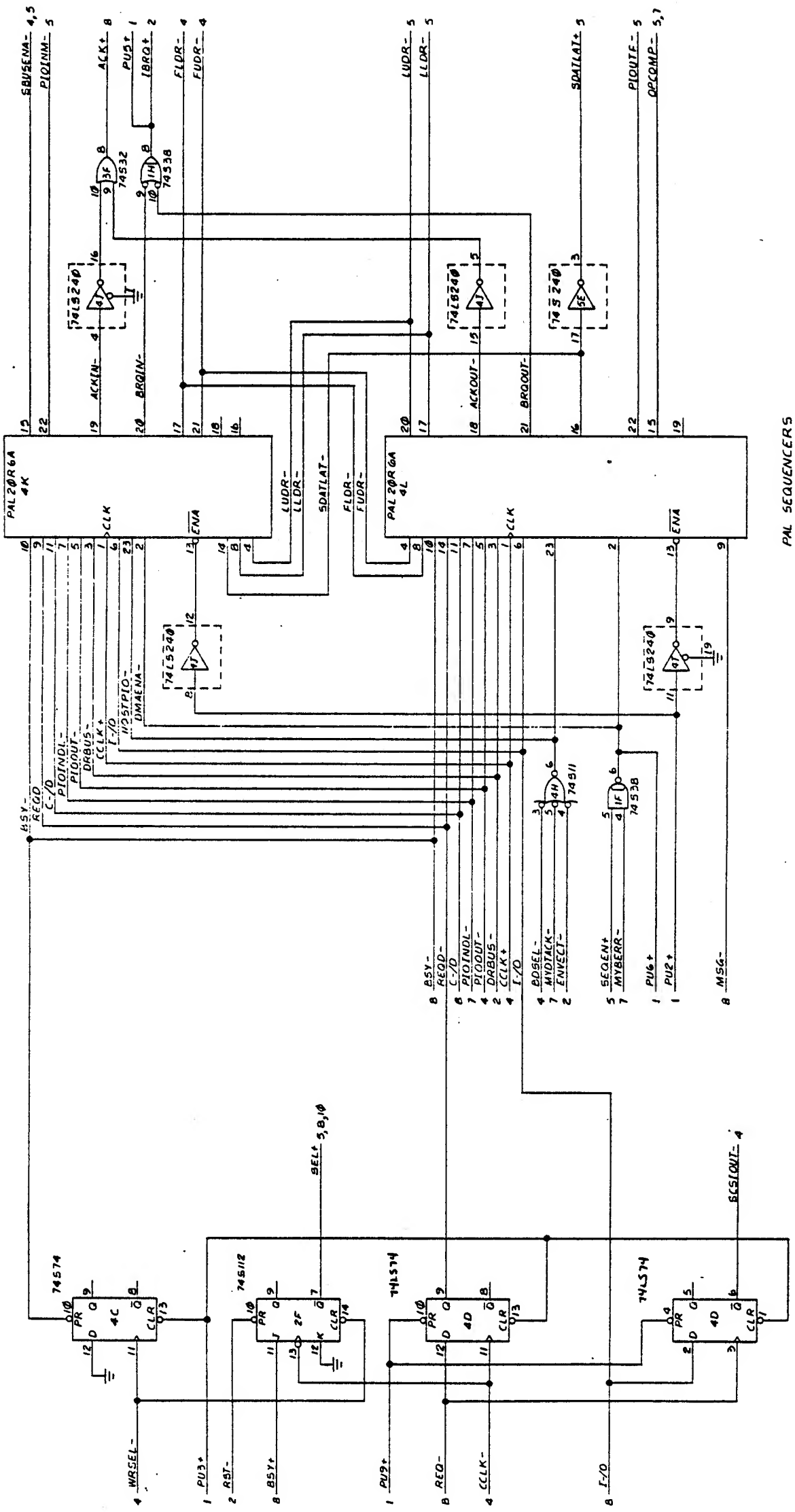


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 5 of 12)



PAL SEQUENCERS

Figure A-10. Part No. 903496, Schematic Diagram (Sheet 6 of 12)

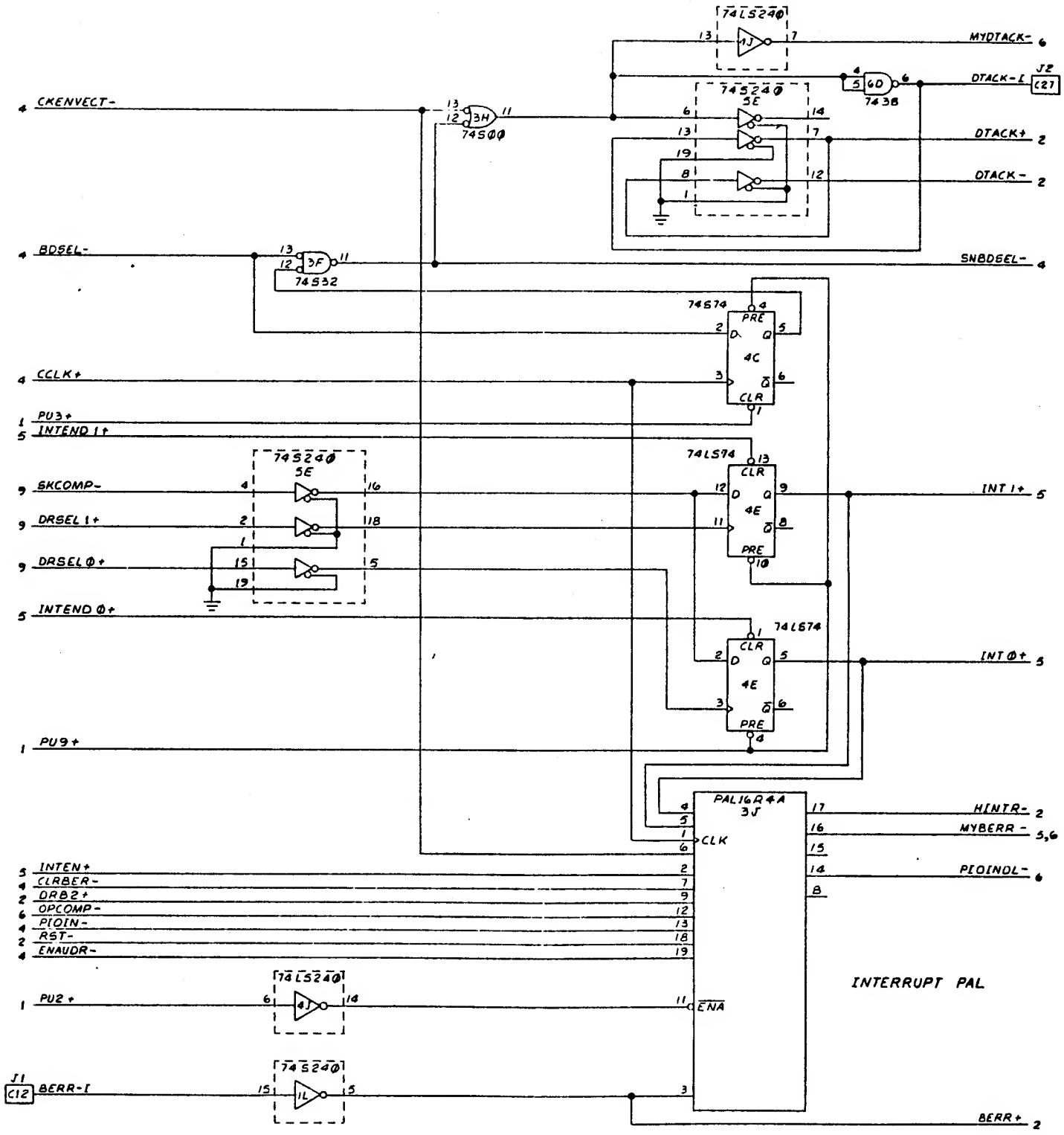


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 7 of 12)

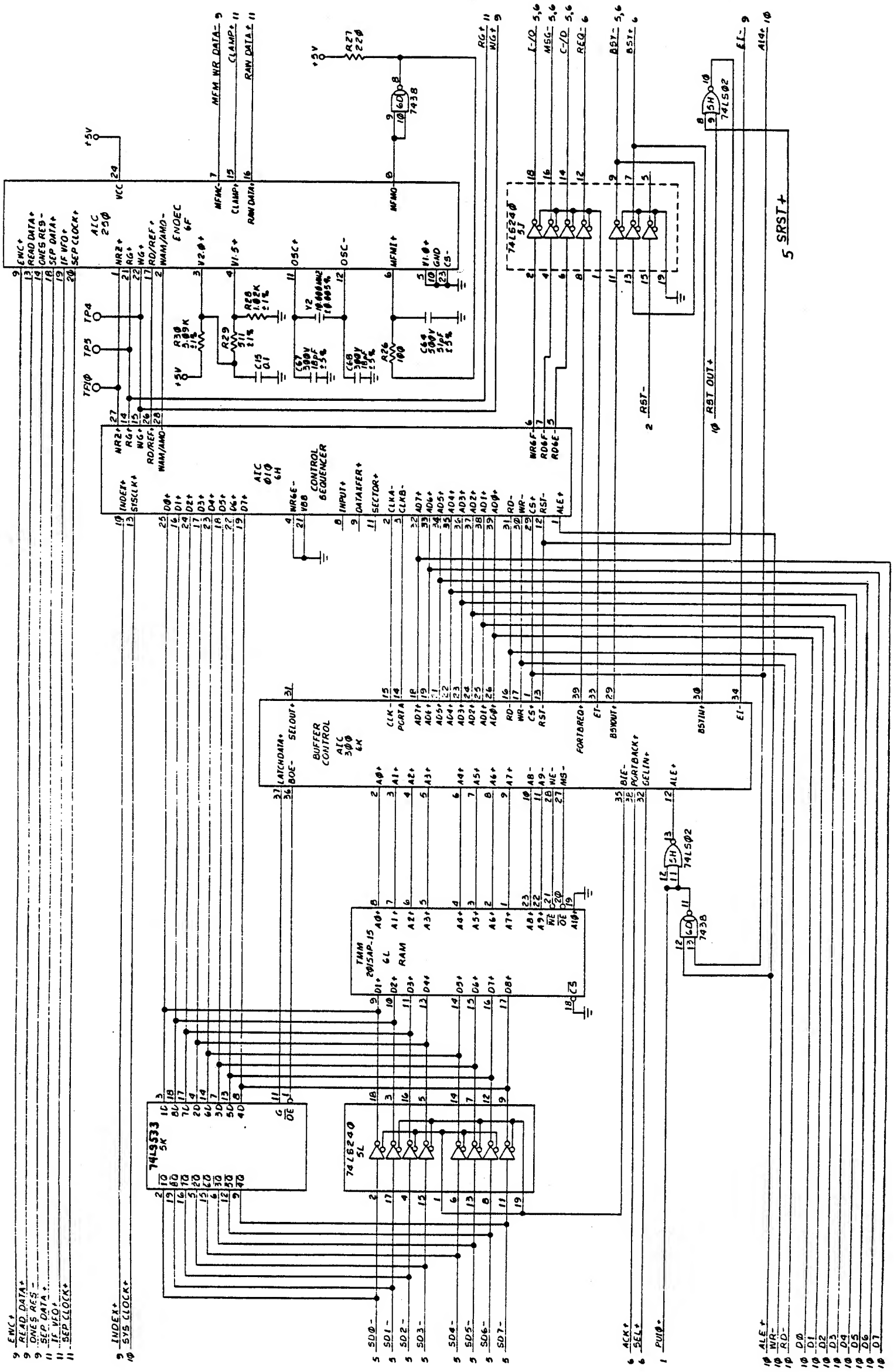


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 8 of 12)

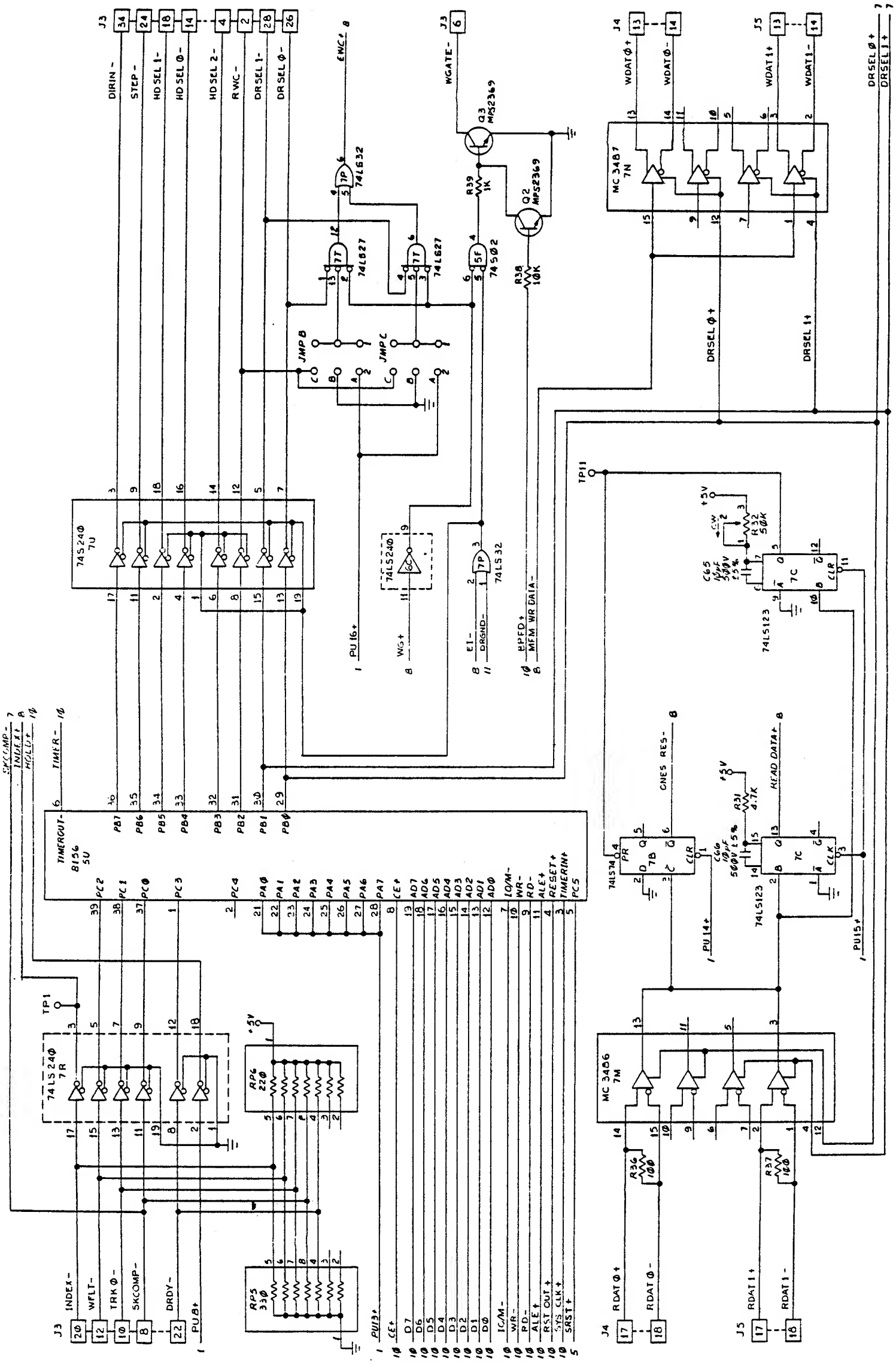


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 9 of 12)

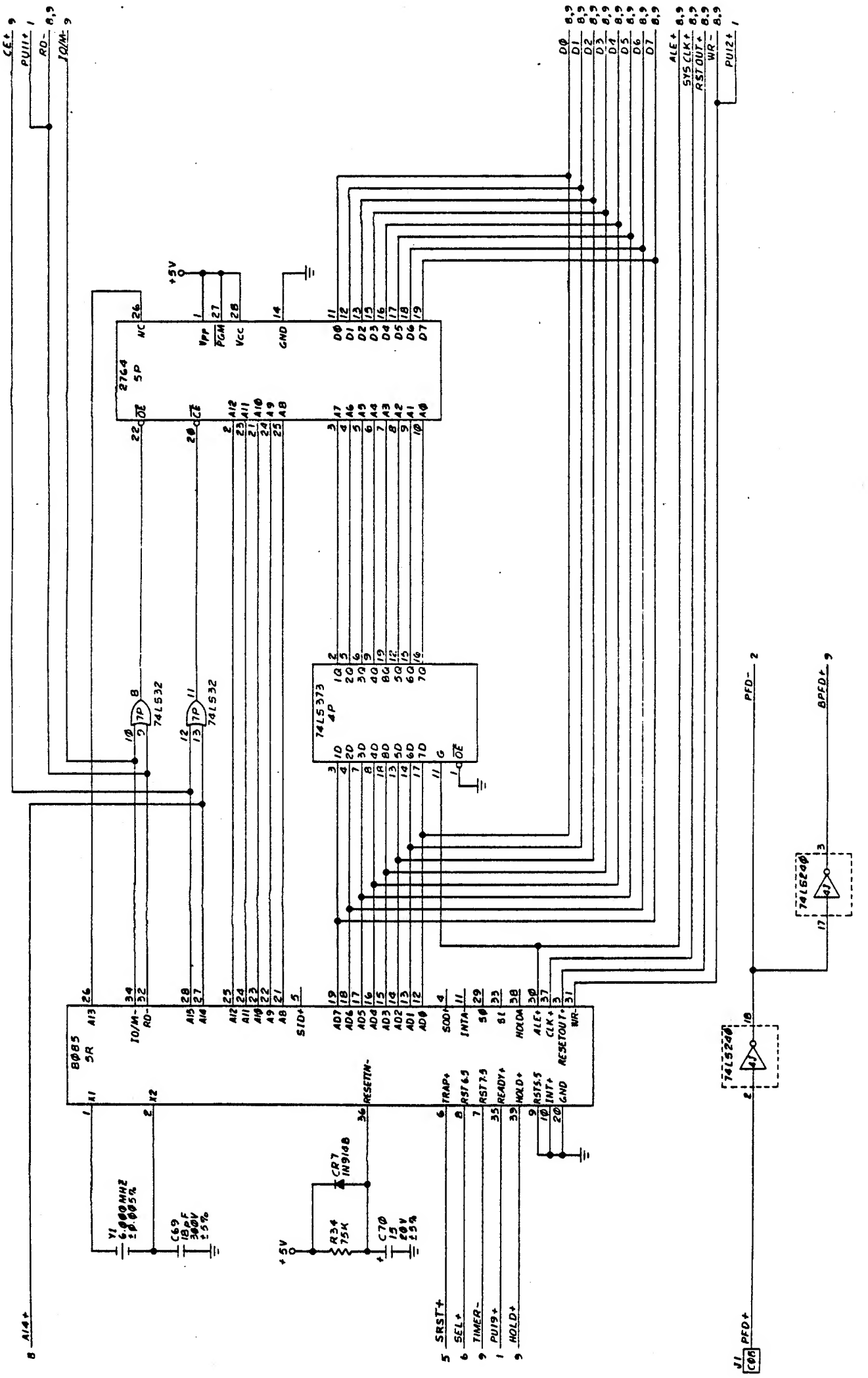


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 10 of 12)

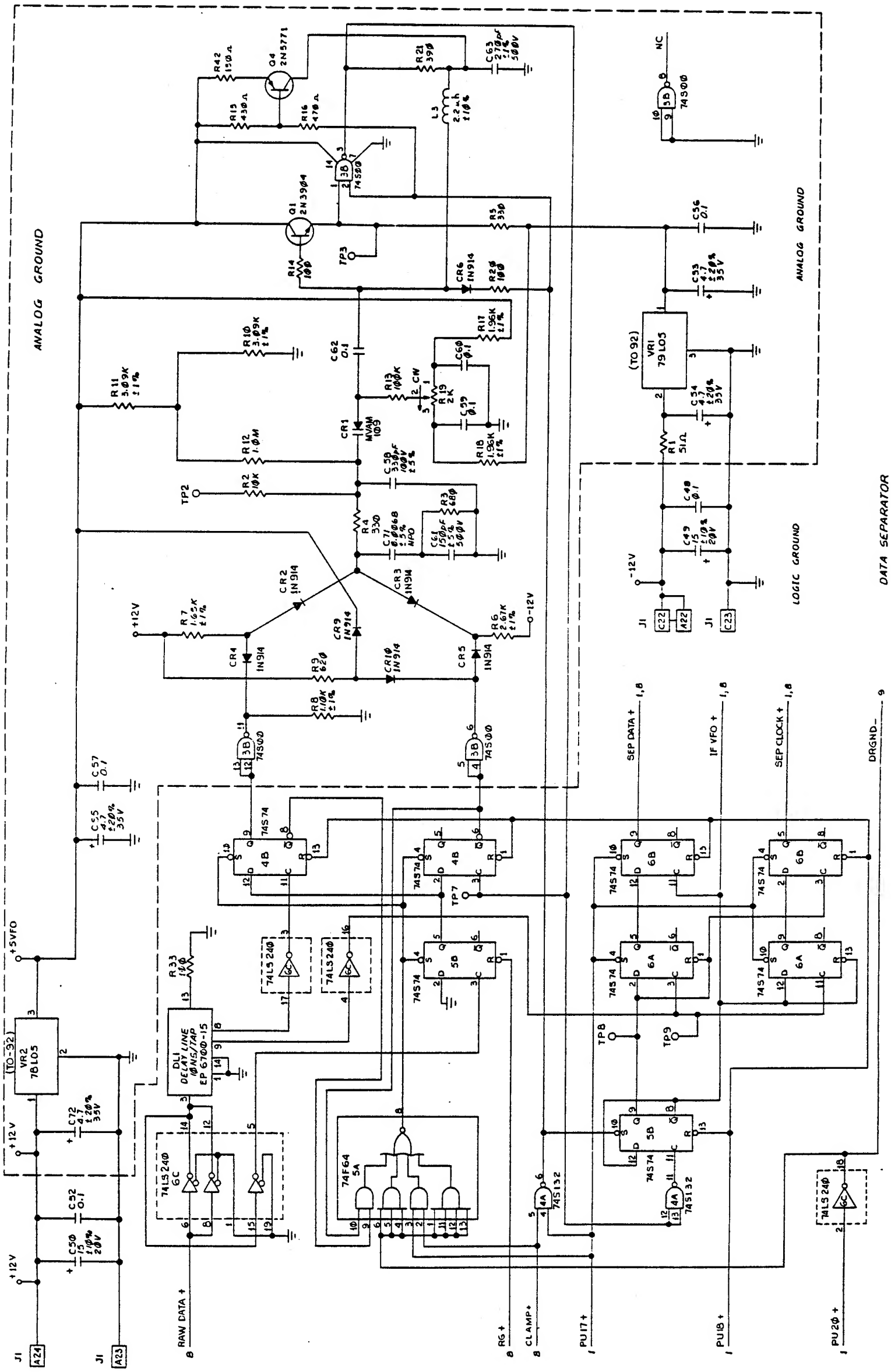


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 11 of 12)

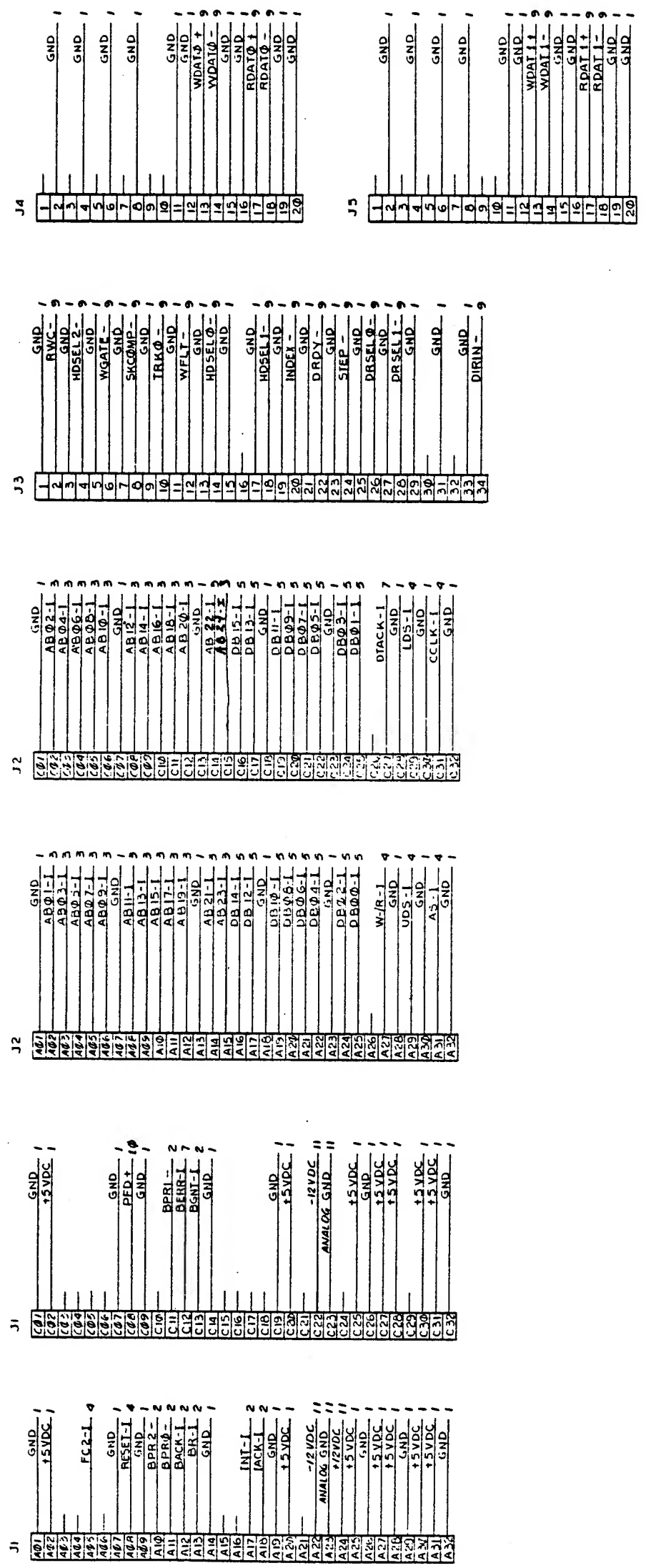


Figure A-10. Part No. 903496, Schematic Diagram (Sheet 12 of 12)

NOTES

NOTES

APPENDIX B

TWO-BOARD WDC MAINTENANCE AIDS

The following Programmed Logic Array (PAL) information, interface data, parts list data and logic diagrams for the WDC Controller, Part No. 903439-001 and SCSI Bus Adapter, Part No. 907649-001 are provided to aid in clarifying the operation of the WDC and assist in the maintenance of the PCBAs:

NOTE

The PAL state diagrams and equations in this appendix are provided for reference purposes only and will not be maintained.

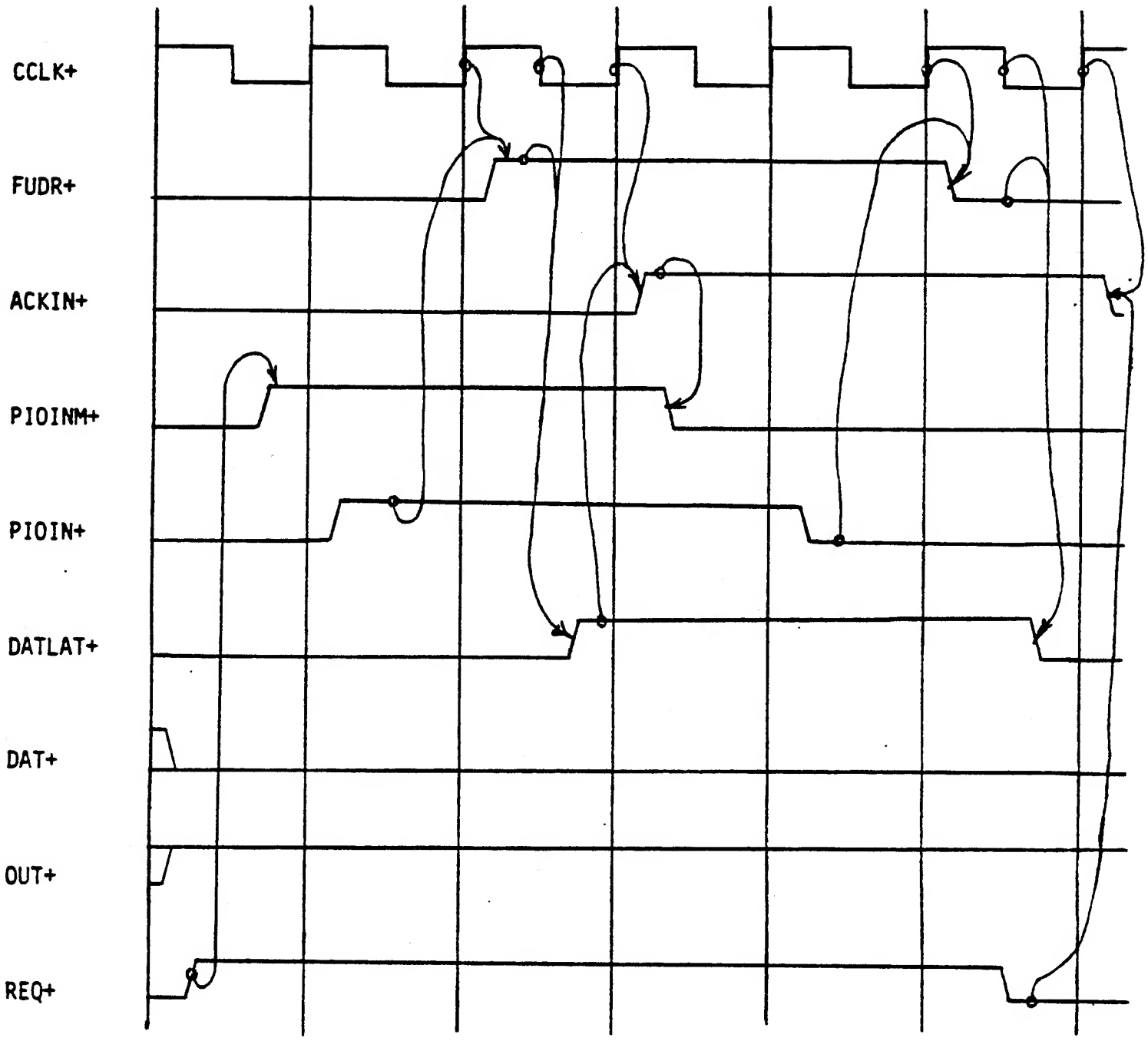


Figure B-1. BOSS IX System to WDC Programmed I/O PAL Timing Diagram

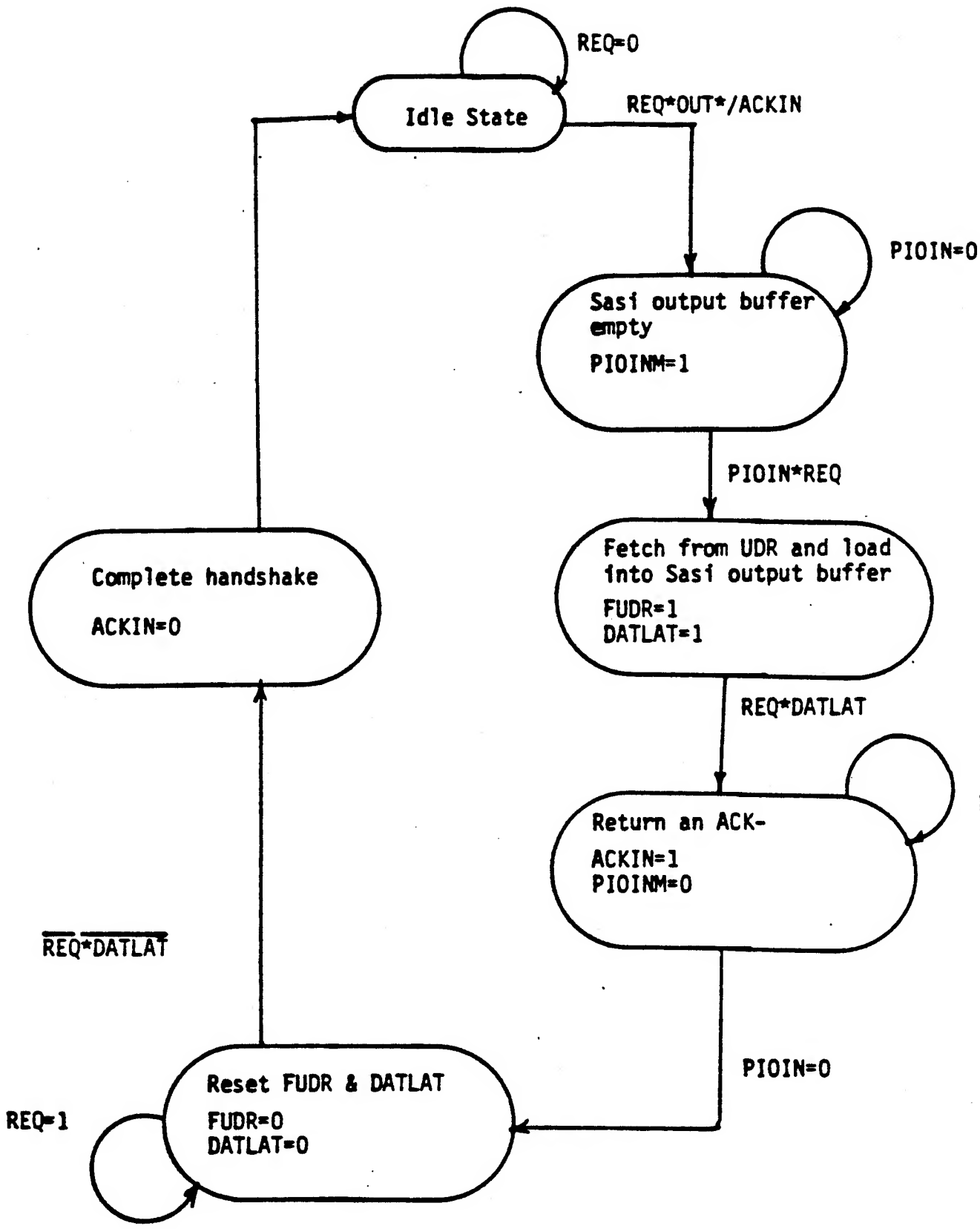


Figure B-2. BOSS IX System to WDC Programmed I/O PAL State Di

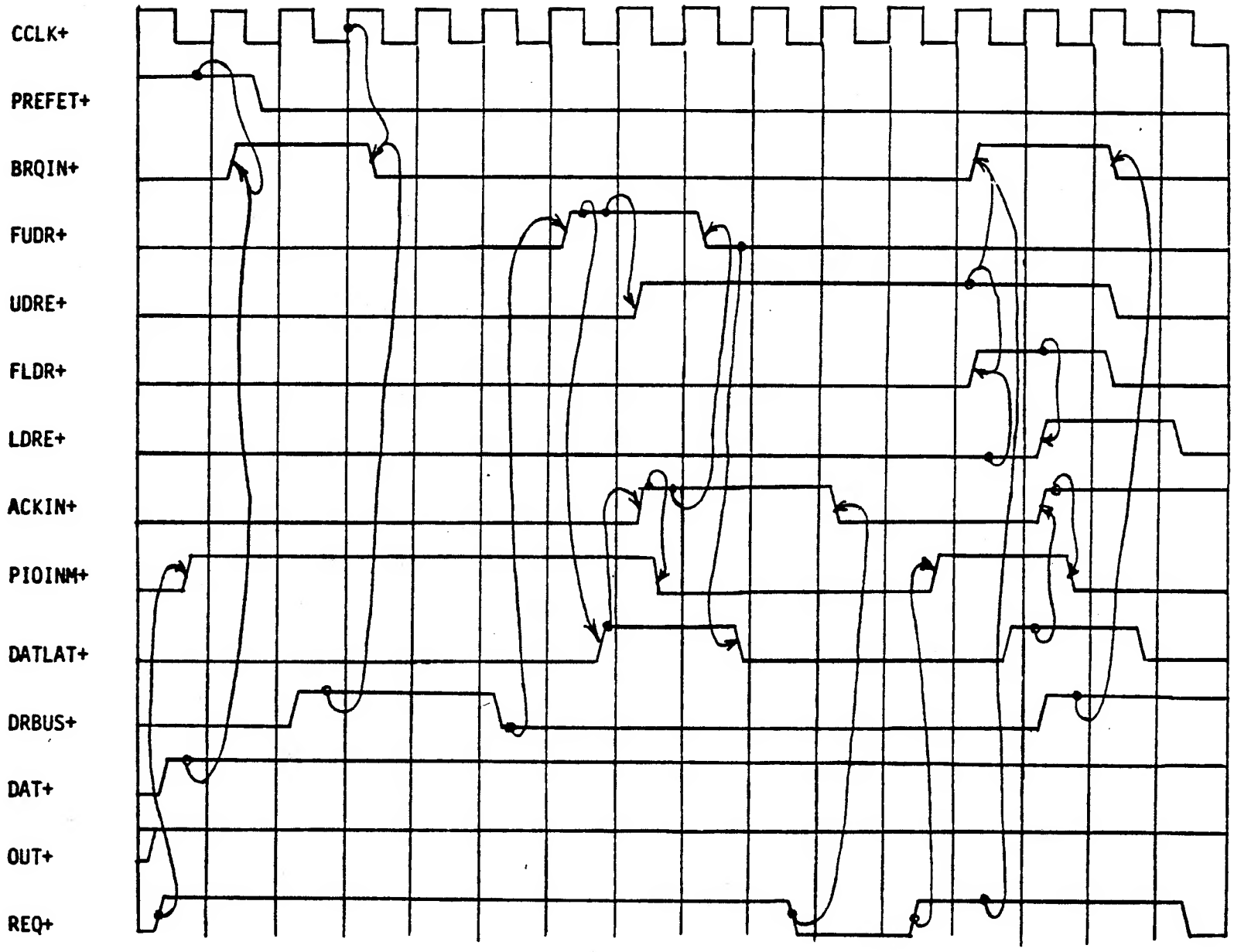


Figure B-3. BOSS IX System to WDC Programmed DMA PAL Timing Diagram

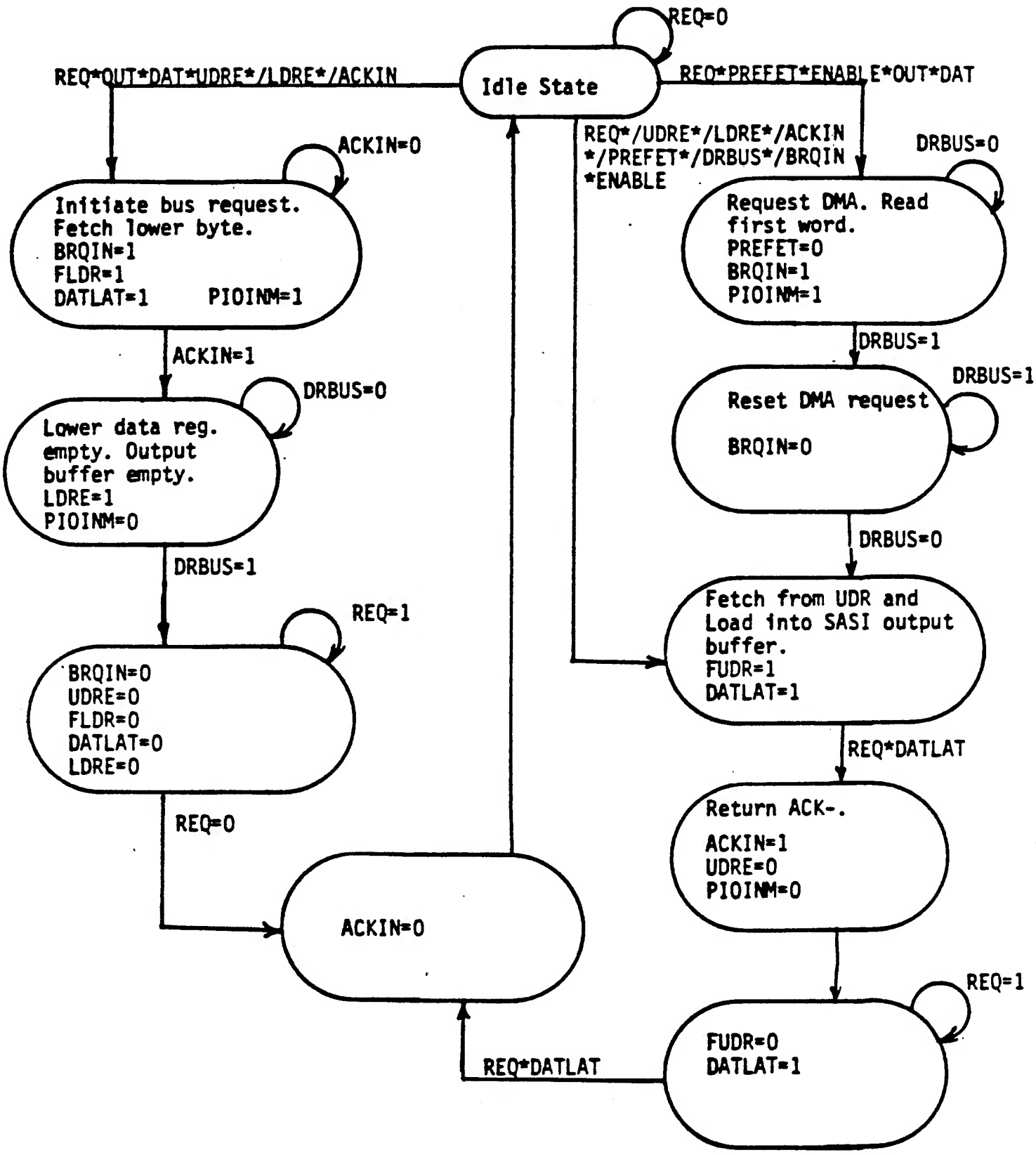


Figure B-4. WDC to BOSS IX System Programmed DMA PAL State Diagram

Table B-1. BOSS IX System to WDC PAL Signal Listing

```
CCLK   BUSY      REQ      /OUT    /DAT    ENABLE   /DRBUS   DATLAT   /PIOIN    GND
/ENB   /PIOINM   /ACKIN   /LDRE   /FLDR   /UDRE    /FUDR    /BRQIN   /PREFET   VCC

PREFET      = /ENABLE
            + PREFET * /BRQIN
            + BUSY

FUDR        := REQ * /UDRE * /LDRE * /PREFET * /DRBUS * /ACKIN * /BRQIN
               * ENABLE * OUT * DAT
            + REQ * PIOIN
            + FUDR * /ACKIN * ENABLE
            + PIOIN * /BUSY * /ENABLE * /LDRE * /FLDR
            + LDRE * /BUSY * /ENABLE * /DRBUS * /UDRE

UDRE        := FUDR * ENABLE * OUT * DAT * /PIOIN * REQ
            + UDRE * ENABLE * /DRBUS * BUSY
            + FUDR * /ENABLE * /BUSY * LDRE
            + UDRE * /ENABLE * /BUSY * /FLDR

FLDR        := REQ * ENABLE * OUT * DAT * UDRE * /LDRE * /ACKIN
            + FLDR * ENABLE * BUSY * /ACKIN
            + PIOIN * /BUSY * /ENABLE * LDRE

LDRE        := FLDR * ENABLE * OUT * DAT * REQ
            + LDRE * ENABLE * /DRBUS * BUSY
            + DRBUS * /BUSY * ENABLE
            + LDRE * /FLDR * /BUSY

ACKIN       := REQ * DATLAT
            + REQ * ACKIN
            + DATLAT * /BUSY

BRQIN       := REQ * PREFET * ENABLE * OUT * DAT
            + REQ * UDRE * /LDRE * OUT * DAT * /ACKIN * ENABLE
            + BRQIN * /DRBUS * ENABLE
            + PIOIN * ENABLE * /BUSY * PREFET

PIOIN       := /REQ
            + /OUT
            + ACKIN
```

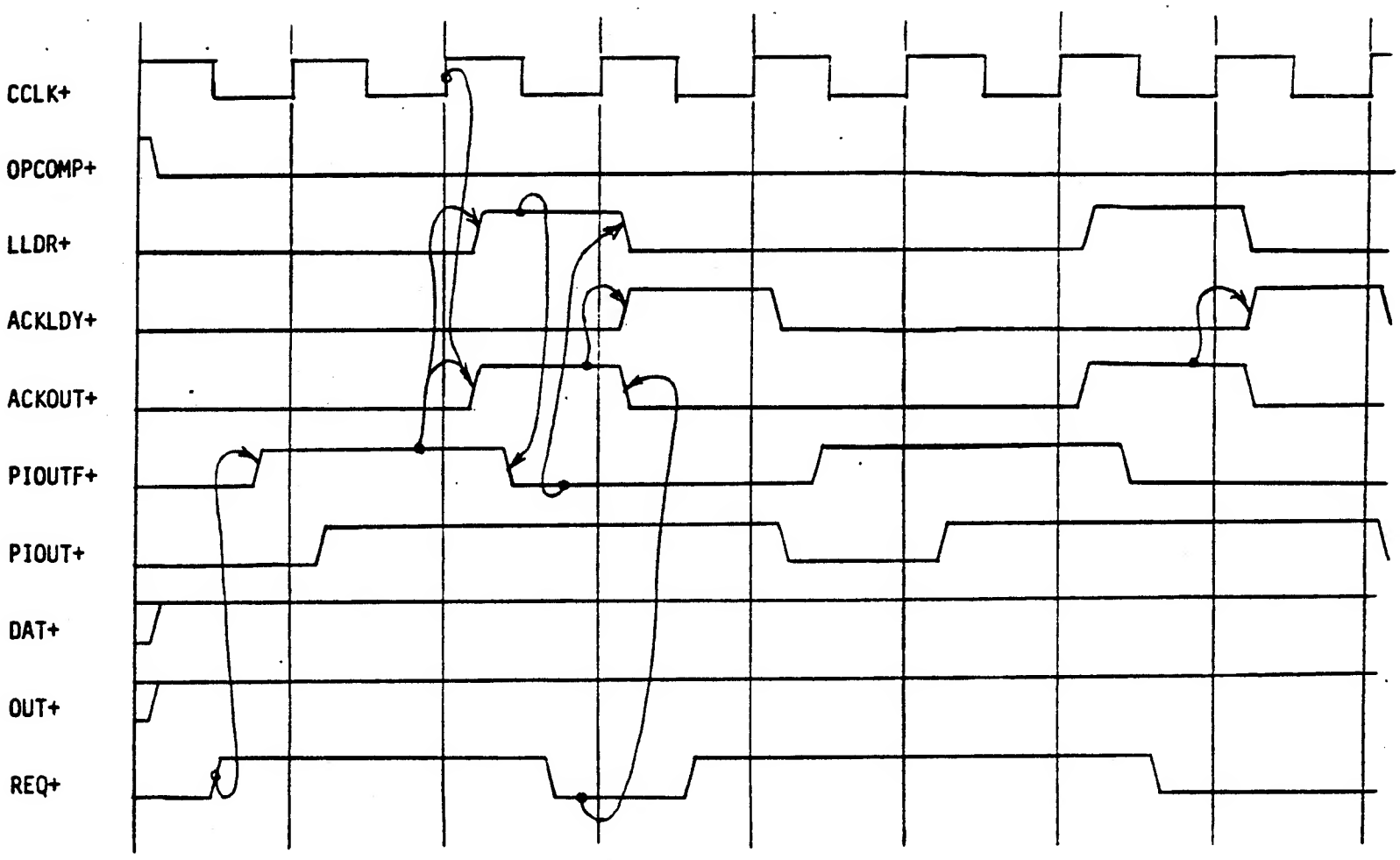


Figure B-5. WDC to BOSS IX System Programmed I/O PAL Timing Diagram

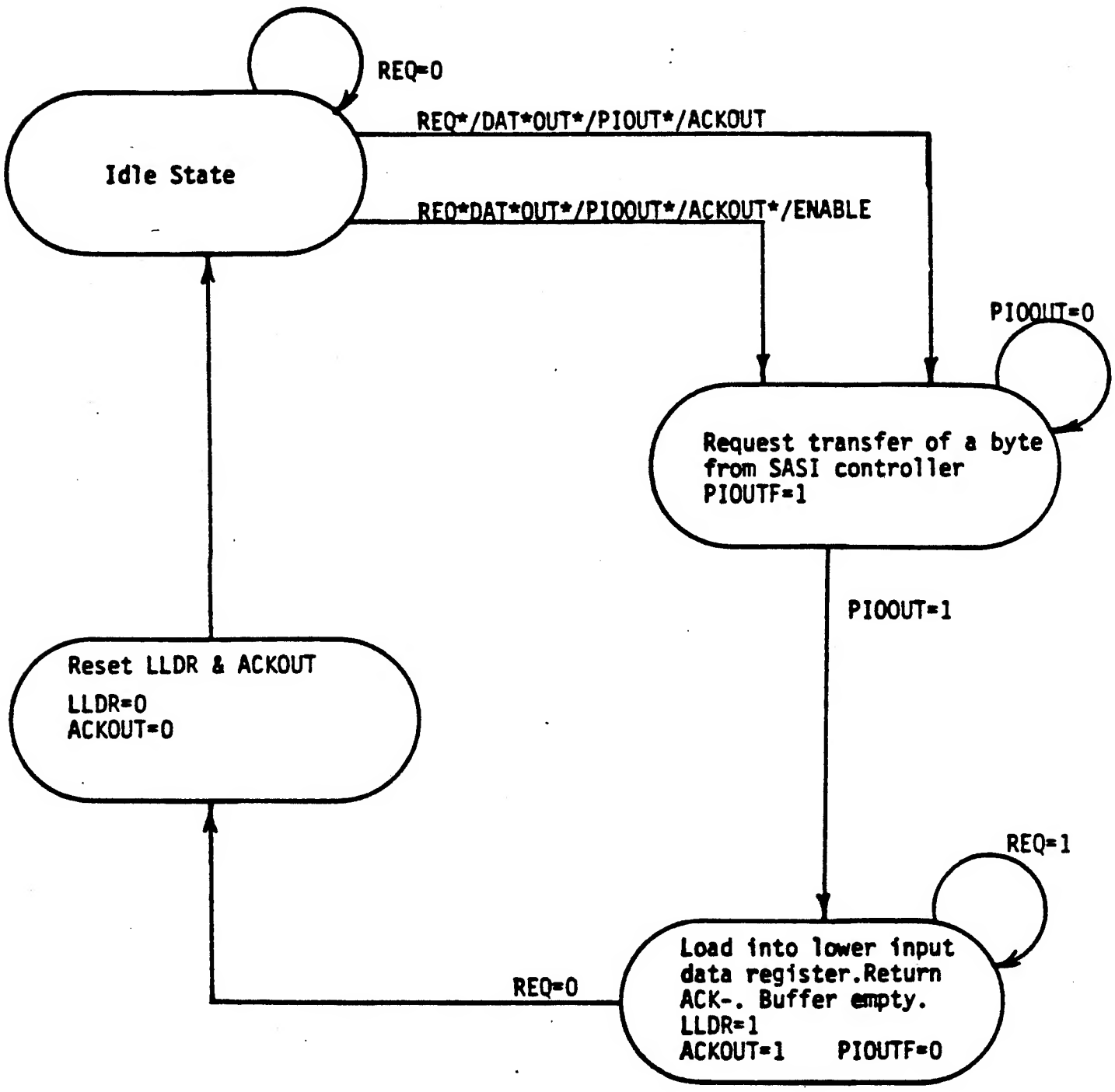


Figure B-6. WDC to BOSS IX System Programmed I/O PAL State Diagram

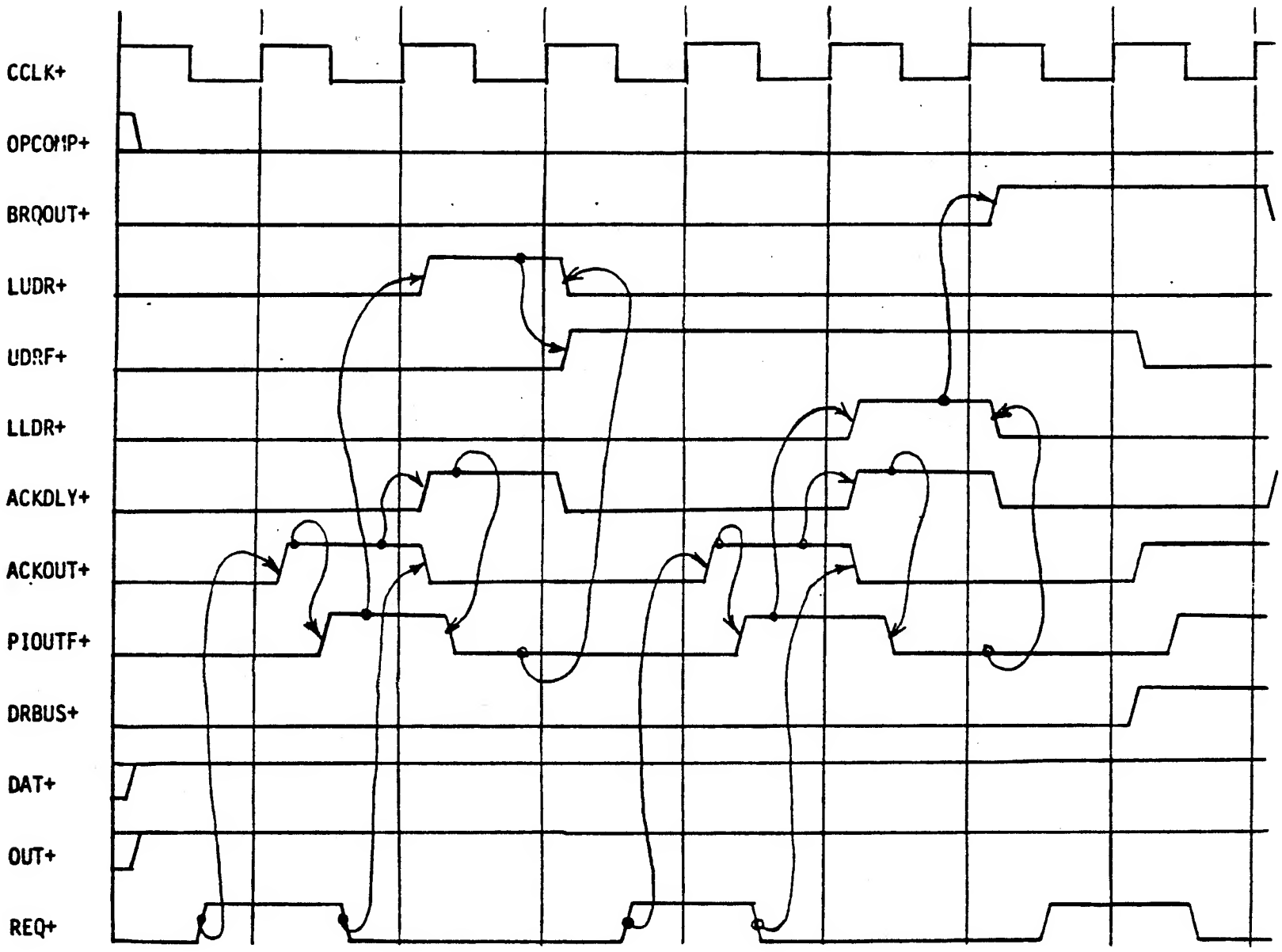


Figure B-7. WDC to BOSS IX System Programmed DMA PAL Timing Diagram

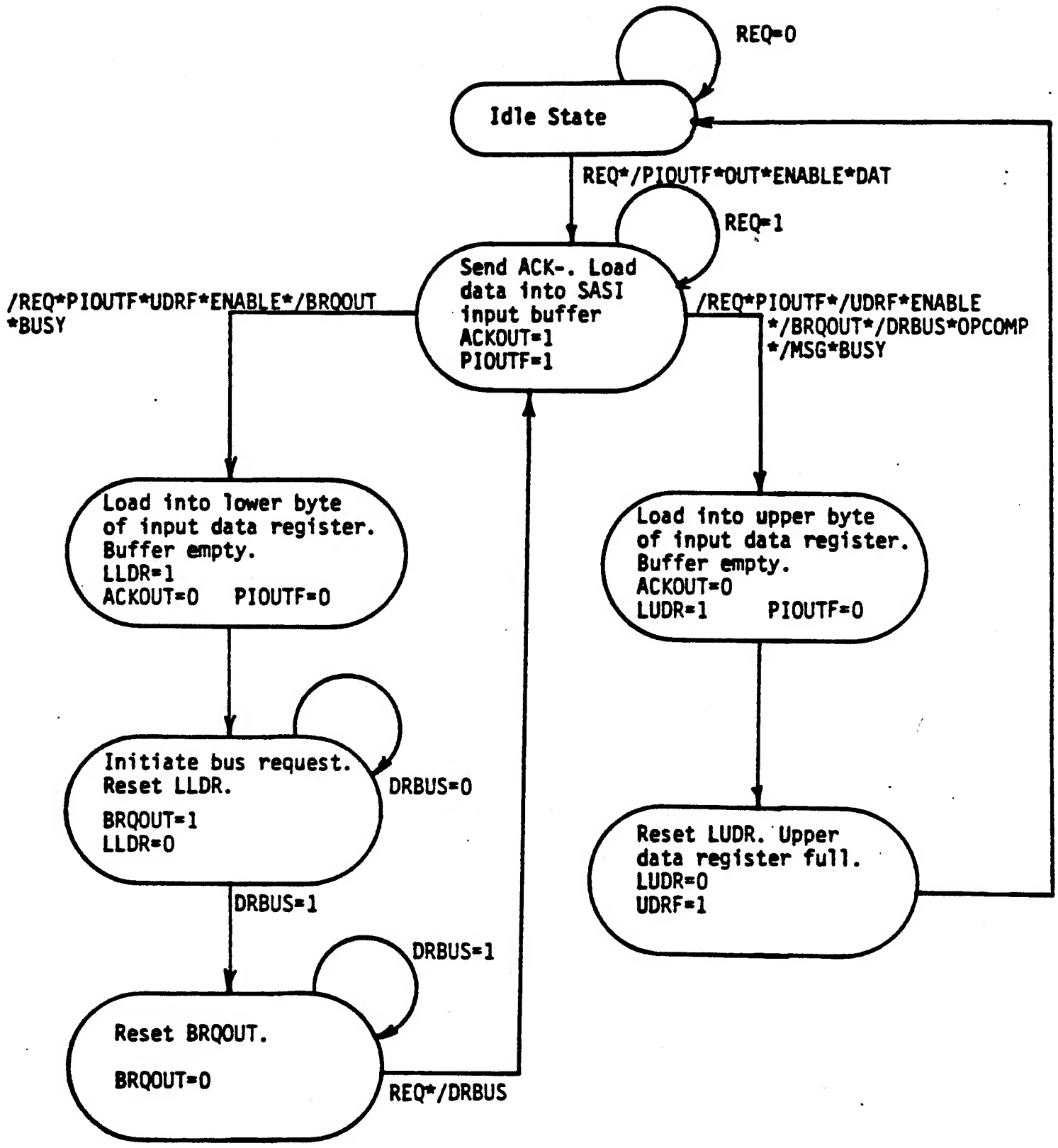


Figure B-8. WDC to BOSS IX System Programmed DMA PAL State Diagram

Table B-2. BOSS IX System I/O Bus (EBUS) Interface Signal Descriptions

SIGNAL	IN/OUT	DESCRIPTIONS
AB00-23	IN/OUT	23-BIT ADDRESS BUS
AS-	IN/OUT	ADDRESS STROBE, TO INDICATE ADDRESS ON THE ADDRESS BUS IS STABLE
BGACK-	IN/OUT	BUS GRANT ACKNOWLEDGE, TO INDICATE BUS CONTROL IS BEING TRANSFERRED
BGNT-	IN	BUS GRANT, TO INDICATE GRANT THE BUS FROM 68000 UP
BERR-	IN	BUS ERROR, TO INDICATE ABNORMAL CONDITION ON THE HOST BUS
BR-	OUT	BUS REQUEST, TO INDICATE ADAPTER IS REQUESTING USAGE OF BUS
BPRO- to BPR3-	OUT	BUS PRIORITIES, ENCODED PRIORITY ADDRESS USED TO RESOLVE PRIORITIES BY BUS MASTER
CCLK-	IN	CPU CLOCK
DB00-15	IN/OUT	16-BIT DATA BUS, USED TO TRANSFER COMMANDS AND DATA

Table B-3. SCSI Interface Signal Descriptions

SIGNAL	IN/OUT	DESCRIPTIONS
I-/O	IN	IN/OUT, TO INDICATE FLOW DIRECTION OF INFORMATION ON THE SASI BUS.
C-/D	IN	COMMAND/DATE, TO INDICATE WHETHER INFORMATION ON THE BUS IS COMMAND OR DATA
BUSY-	IN	BUSY TO INFORM ADAPTER THAT CONTROLLER IS READY TO CONDUCT TRANSACTIONS
MSG-	IN	MESSAGE, TO INDICATE THAT SASI BUS IS IN THE MESSAGE PHASE
REQ-	IN	REQUEST, TO REQUEST A BYTE FROM ADAPTER OR TO INDICATE THAT DATA ON BUS IS STABLE
ACK-	OUT	ACKNOWLEDGE, TO INDICATE TO CONTROLLER THAT ADAPTER HAS ALREADY TAKEN A BYTE OR THAT DATA ON THE BUS IS STABLE
RST-	OUT	RESET, TO FORCE THE CONTROLLER INTO AN IDLE STATE
SEL-	OUT	SELECT, TO INITIATE A COMMAND TRANSACTION
DB7- to DB0-	IN/OUT	8-BIT DATA BUS, USED TO TRANSFER COMMANDS AND DATA

Table B-4. List of WDC Mnemonics

SIGNAL NAMES	DESCRIPTION
AB01-23	EBUS ADDRESS BUS BITS 01 THROUGH 23
ACKIN	ACKNOWLEDGE DATA IN TO CONTROLLER
ACKOUT	ACKNOWLEDGE DATA OUT FROM CONTROLLER
BD0-15	BUFFERED DATA BITS 0 THROUGH 15
BERR	EBUS BUS ERROR
BG	EBUS BUS GRANT
BACK	EBUS BUS GRANT ACKNOWLEDGE
CCLK	HOST CPU CLOCK
CLRBER	CLEAR BUS ERROR LATCH
DATLAT	DATA LATCH
DB00-15	EBUS DATA BUS BIT 00 THROUGH 15
DBDIR	DATA BUS DIRECTION
DMADRL	LOAD LOWER DMA ADDRESS REGISTER
DMADRM	LOAD MIDDLE DMA ADDRESS REGISTER
DMADRH	LOAD HIGHER DMA ADDRESS REGISTER
DRBUS	DRIVE EBUS
DTACK	EBUS DATA TRANSFER ACKNOWLEDGE
ENVECT	ENABLE VECTOR ONTO EBUS
FC2	EBUS FUNCTION CODE BIT 2
FLDR	FETCH FROM LOWER BYTE OF DATA REGISTER

PAD ISOLATION CHART		
CUT NO.	LOCATION	REMARKS
1	5K-9	COMP SIDE

JUMPER WIRE CHART			
JUMP NO.	FROM	TO	REMARKS
1	5K-9	2H-6	COMP SIDE
2	1P-10	1N-10	COMP SIDE
3	5D-7	5D-8	COMP SIDE, LOCATION
			PIN 8, NOT I.C. PIN 8

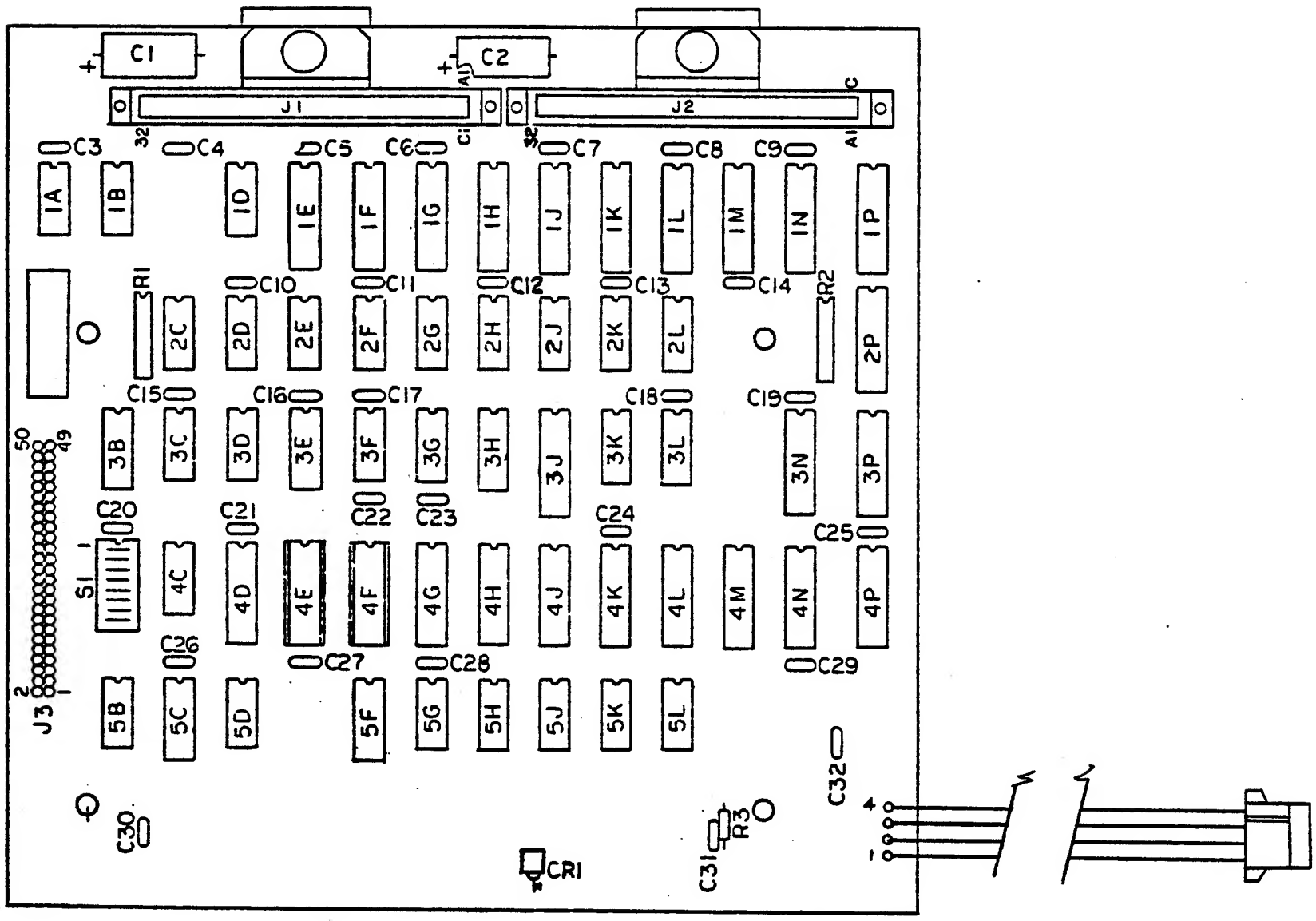


Figure B-9. Part No. 903439-001, Parts Location Diagram

Table B-5. Part No. 903439-001, List of Parts (Sheet 1 of 2)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0001	904854-001	PCB WDC BUS ADAPTER	*
0003	762022-003	LABEL TAB .375X1.250 YEL	*
0005	101514	IC 7438 BUFFER QUAD 2 INPUT NAND	5B
0007	101709	IC 74LS00 QUAD 2-IN NAND	5H,5J
0008	101710	IC 74LS02 QUAD 2 IN NOR	3K
0009	101711	IC 74LS08 QUAD 2INP AND	3L,5K
0010	101656	IC 74LS04 HEX INVERTER	5G
0011	161015	IC 74LS14 HEX SCHMITT TRIGGER INVERTER	4C
0014	101740	IC 74LS51 DUAL 2-WIDE 2-IN-&/OR-INVERT	1D
0015	101741	IC 74LS74 DUAL D-TYPE POS EDG-TRIG F/F	3F
0018	101719	IC 74LS138 3-8 LINE DECODER/DMLTPLXR	3H
0021	101633	IC SN74S157 QUAD 2-1 LINEDATA SLCT/MUX	3B
0022	161068-001	IC 74LS244 OCTAL BUFFER/LINE DRIVER	4L,4P
0024	161064-001	IC 74LS240 BUFF LINE DR 3-ST OCTAL	1E,3J
0026	161023	IC 74LS273 OCTAL D-TYPE FLIP-FLOP	4J
0027	161065-001	IC 74LS374 OCTAL REGISTER D-TYPE F/F	3N,3P,4G,4H, 4K,4M,4N
0029	161111-001	IC 74LS640 OCTAL BUS TRANS INV 3 STATE	1K,1L,4D
0030	161145-001	IC 74LS697 SYNC U/D BINARY COUNTER	1J,1M,1N,1P, 2P
0033	101315	IC 74S00 QUAD 2 INPUT POS NAND GATE	5L
0034	101655	IC 74S02 POS-NOR GATE TOTEM-POLE	2D,3C
0035	101623	IC-74S11 3 INPUT AND	3G
0036	101625	IC 74S32 QUAD 2 INPUT POSITIVE-OR GATE	2K
0037	101627	IC SN74S38 QUAD 2 INPUT POS NAND BFFR	1A,2F
0038	101615	IC 74S08 QUAD 2 INPUT POS AND GATE	2L
0039	101628	IC 74S64 4-2-3-2 INPUT AND/OR INV GATE	1B
0041	101629	IC SN74S74 DUAL D-TYPE FLIP/FLOP	2C,2H,3D,5D
0043	101630	IC 74S112 DUAL J-K EDGE TRIG FLIP/FLOP	3E,5F
0044	161076-001	IC 74S133 13 INP NAND	2G
0045	101631	IC 74S138 DECODER/DEMULTIPLEXER	2J
0046	161009	IC 74S240 OCTAL BUFFER 3-STATE TTL	1F,1G
0047	101637	IC SN74S260 DUAL 5 INPUT POS-NOR GATE	2E
0048	161074-001	IC 74S244 OCTAL BUFFER	1H
0055	911006-008	IC PAL WDC CONTROLLER/HOST SEQUENCER	4E
0056	911009-004	IC PAL WDC HOST/CONTROLLER SEQUENCER	4F
0061	119016-003	RES NTWK SIP C/C 8 PIN 7 RES 1.0K OHM	R1,2
0062	119009-004	RES NTWK DIP 16 PIN 28 RES 220/330 OHM	5C
0075	104010-001	CAP CERAM Z5U AXIAL .1UF +80 -20% 50V	C3-32
0076	108016-004	CAP ALUM ELECT 100UF +75 -20% 6V	C1,2
0080	300092-001	CONN DIN FML 3X32 PRESS-FIT 64 POS A&C	J1,2
0081	310019-001	CONN HOUSING/GUIDE DIN 3X32 .100CTS ML	(J1,2)
0082	300032-012	CONN HDR DBL ROW .100CTS .025SQ 50 POS	J3
0084	907388-001	EJECTOR EURO-DIN CONN STACK	(J1,2)
0085	907769-001	LATCH EURO-DIN CONNECTOR STACK	(J1,2)
0086	907985-001	CATCH PCBA STACK CONTROLLERS	(J1,2)
0087	214027-001	FASTENER PUSH-ON .312 DIA STUD	(J1,2)
0090	325005-011	SOCKET IC DIP 4-LEAF CONT GOLD 20 POS	(4F,4E)
0095	331014-005	SWITCH DIP SLIDE SPST AUTO-INSERT 8SEC	(4B)

Table B-5. Part No. 903439-001, List of Parts (Sheet 2 of 2)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0096	152001-001	DIODE LIGHT EMITTING GREEN DIFF LENS	CR1
0097	111000-029	RES CARBON FILM .25W 5% 330OHM	R3
0098	216021-004	STANDOFF INS .62L SNAP-IN	*
0099	907634-001	CBL ASSY DC PWR WDC BUS ADAPTOR/WDC	*

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R3	
C32	
CR1	

POWER CHART (UNLESS OTHERWISE SPECIFIED)					
DEVICE	+5V/+5VB . ⟨4⟩	GND	+12V	-12V	-5V
ALL 20 PIN	20	10			
ALL 16 PIN	16	8			
ALL 14 PIN	14	7			

Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 1 of 13)

COMPONENT MAP

1A	74S38	4	4	4	
1B	74S64	4			
1C	SPARE				
1D	74LS51	5			
1E	74LS240	5	5	5	5
		6	6	11	11
1F	74S240	6	6	6	6
		6	6		
1G	74S240	6	6	6	6
		8	8	8	
1H	74S244	6	6	6	6
		6	8	8	8
1J	74LS697	8			
1K	74LS640	9			
1L	74LS640	7			
1M	74LS697	8			
1N	74LS697	8			
1P	74LS697	8			
2C	74S74	4	4		
2D	74S02	4	5	5	5
2E	74S260	5	5		
2F	74S38	5	5	5	6
2G	74S133	6			
2H	74S74	11	11		
2J	74LS138	6			
2K	74S32	6	6	7	7
2L	74S08	7	8	8	8
2P	74LS697	8			
3B	74S157	4			
3C	74S02	4			
3D	74S74	5	5		
3E	74S112	5	5		
3F	74LS74	10	10		
3G	74S11	4	10	11	
3H	74LS138	6			
3J	74LS240	6	6	6	6
		6	6	6	6
3K	74LS02	7	11		
3L	74LS08	6	7	9	
3M	SPARE				

3N	74LS374	7			
3P	74LS374	9			
4B	SWITCH	4			
4C	74LS14	10	10	10	10
		10			
4D	74LS640	10			
4E	PAL	11			
4F	PAL	11			
4G	74LS374	10			
4H	74LS374	10			
4J	74LS273	9			
4K	74LS374	9			
4L	74LS244	11	11	11	11
		11	11	11	11
4M	74LS374	9			
4N	74LS374	7			
4P	74LS244	9	9	9	9
		9	9	9	9
5B	7438	10	10	10	10
5C	RES NTWK	10			
5D	74S74	11			
5E	SPARE				
5F	74S112	4	10		
5G	74LS04	7	9	11	11
5H	74LS00	6	10	11	
5J	74LS00	6	9	10	
5K	74LS08	11	11	11	11
5L	74S00	5			
5M	SPARE				
5N	SPARE				
6C	SPARE				
6D	SPARE				

6E	SPARE				
6F	SPARE				
6G	SPARE				
6H	SPARE				
6J	SPARE				
6K	SPARE				
6L	SPARE				

Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 2 of 13)

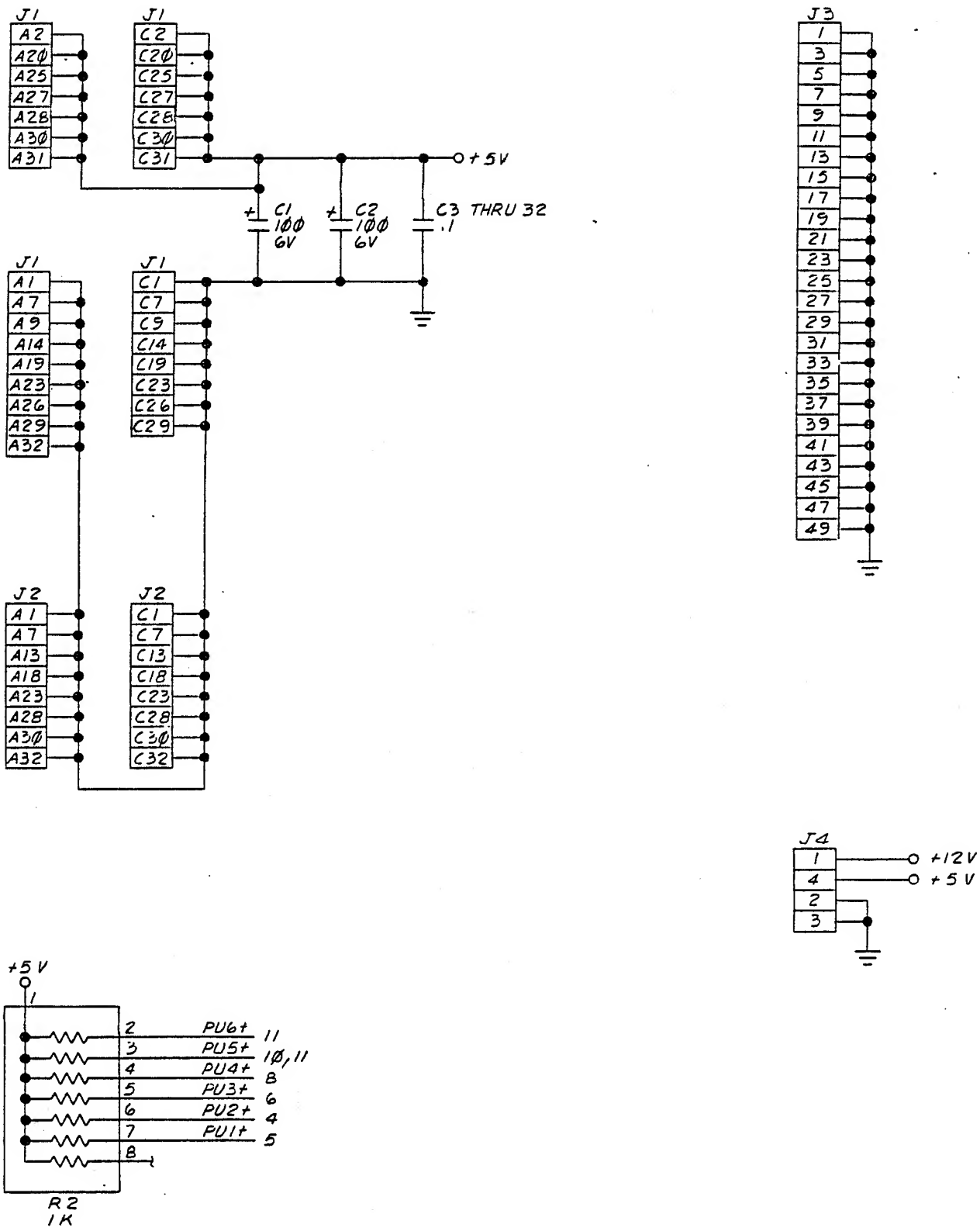


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 3 of 13)

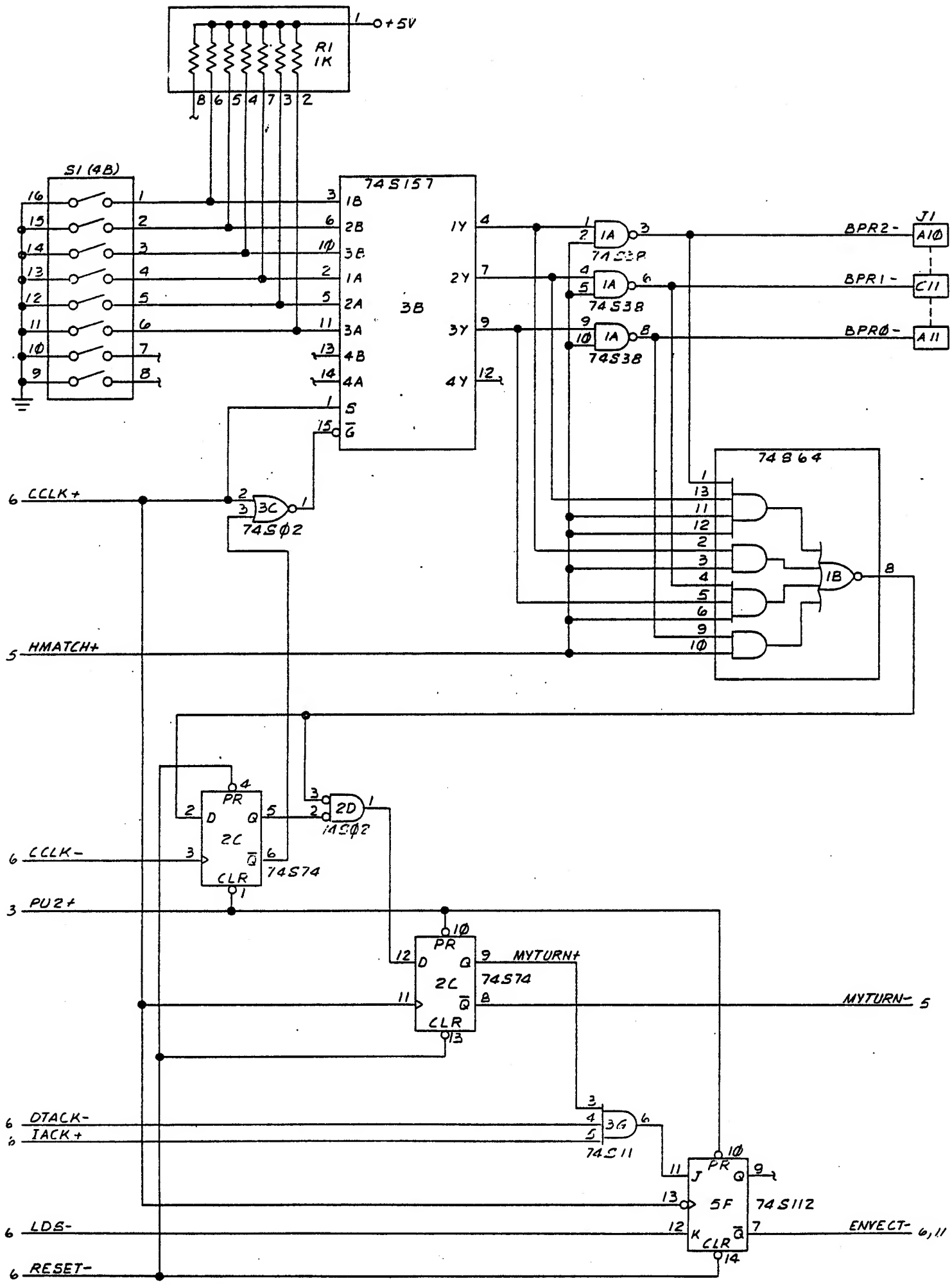


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 4 of 13)

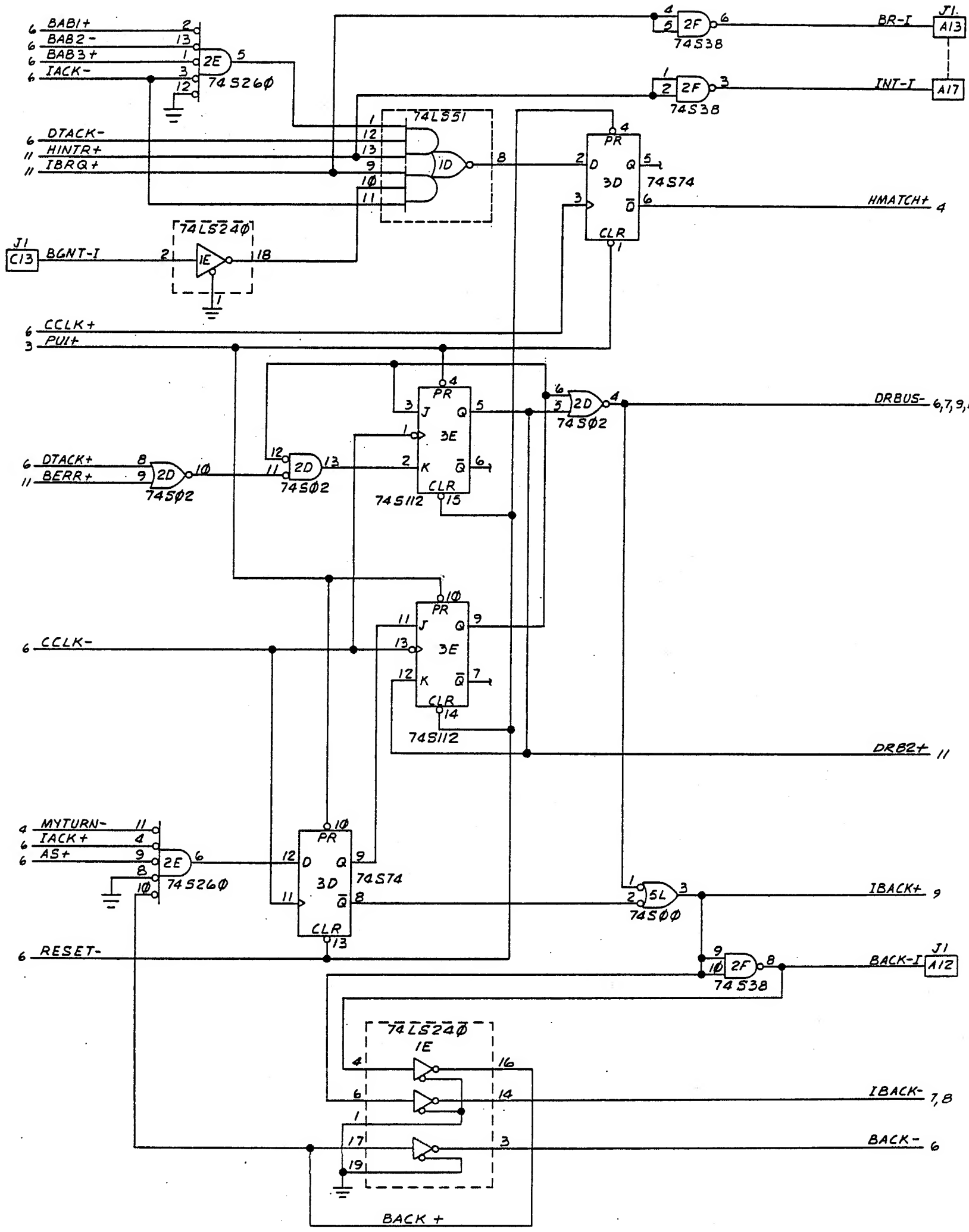


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 5 of 13)

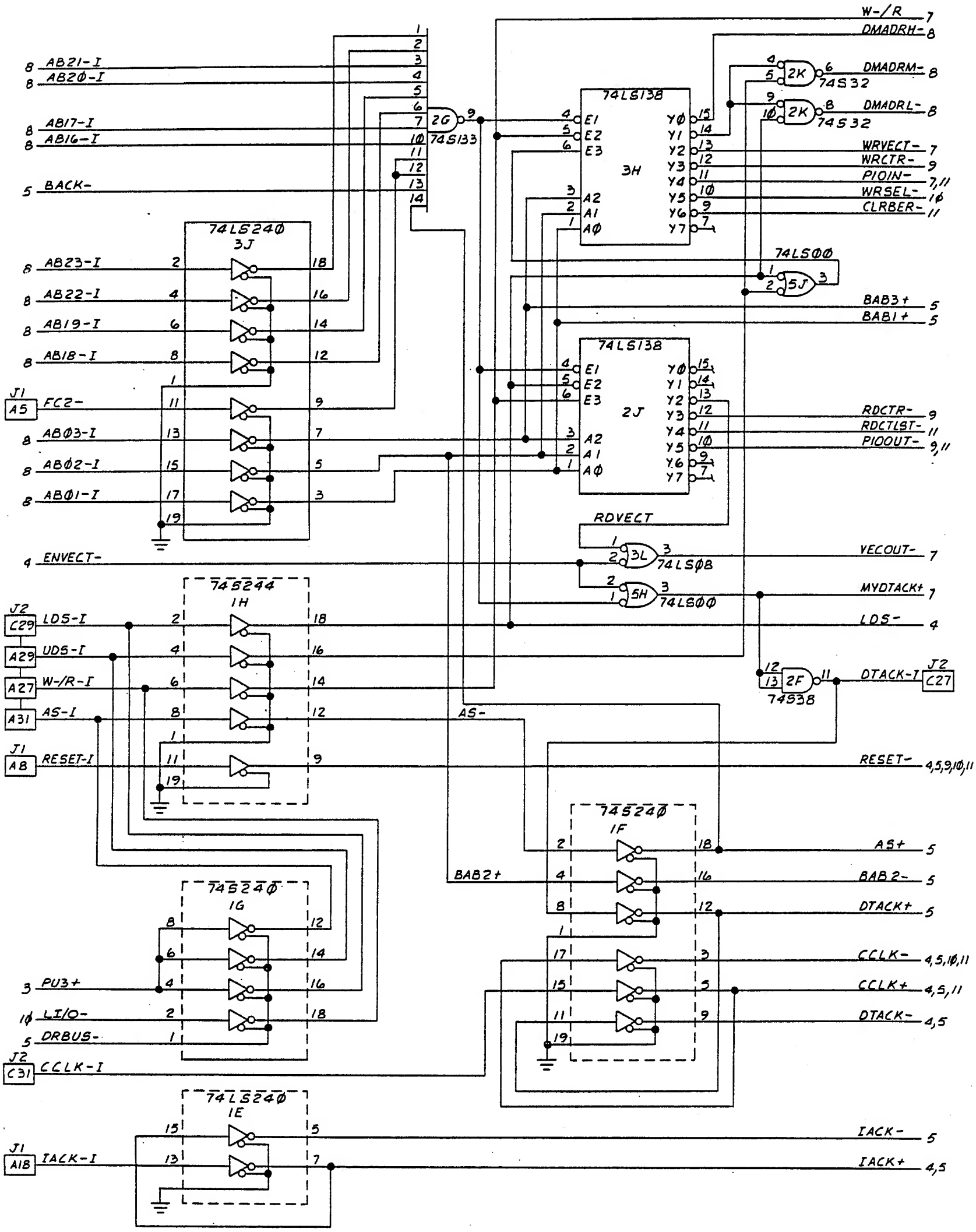


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 6 of 13)

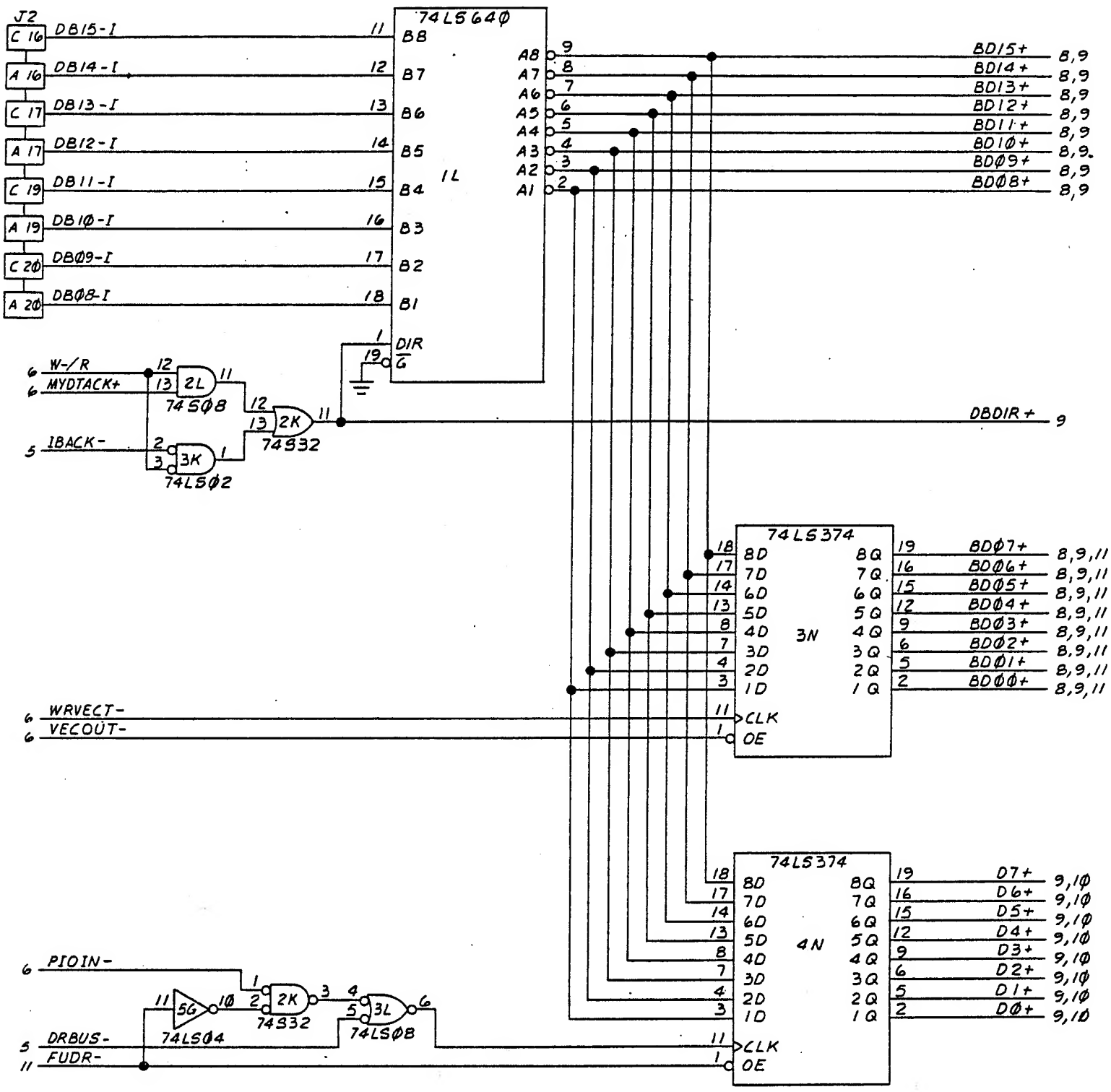


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 7 of 13)

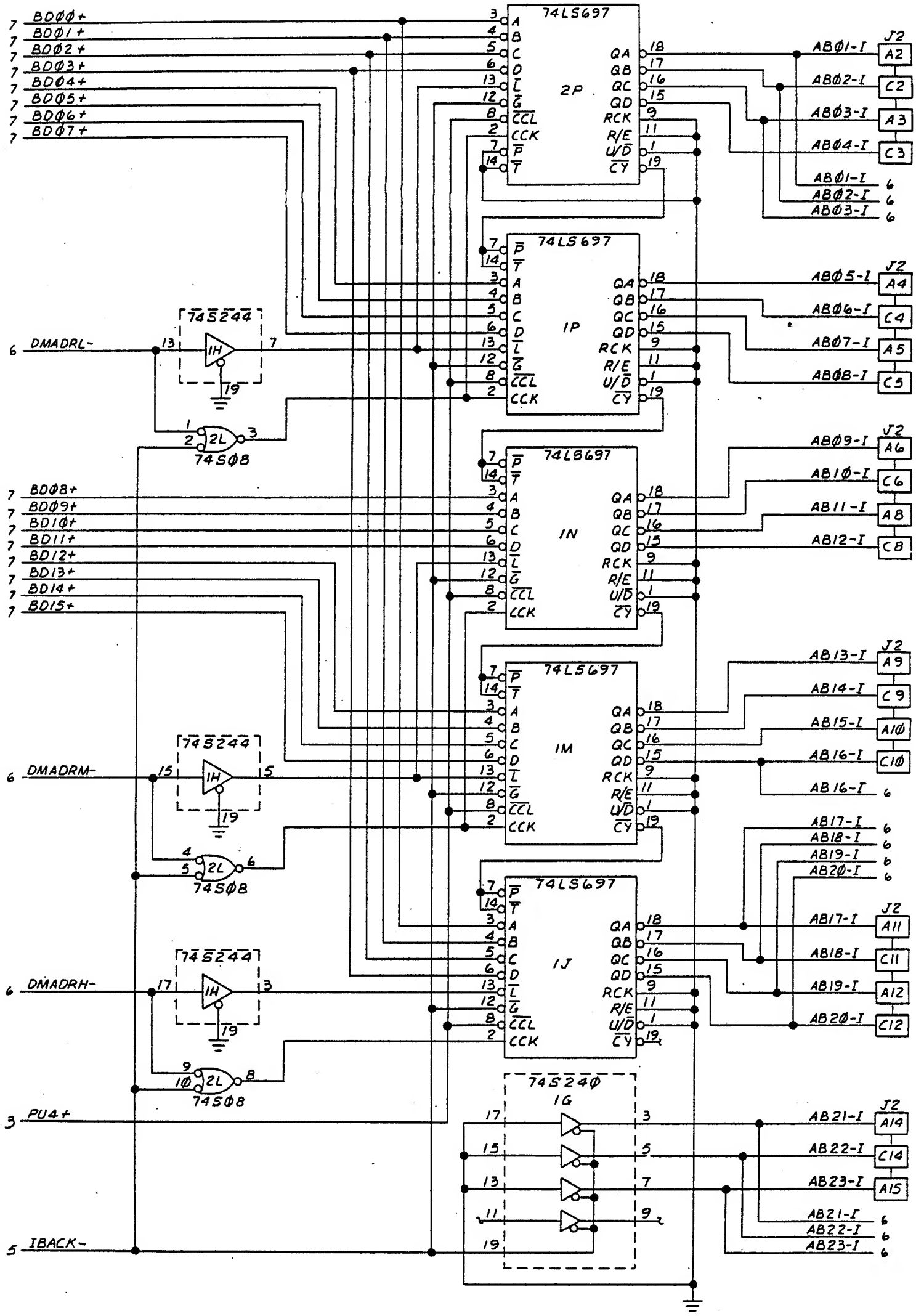


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 8 of 13)

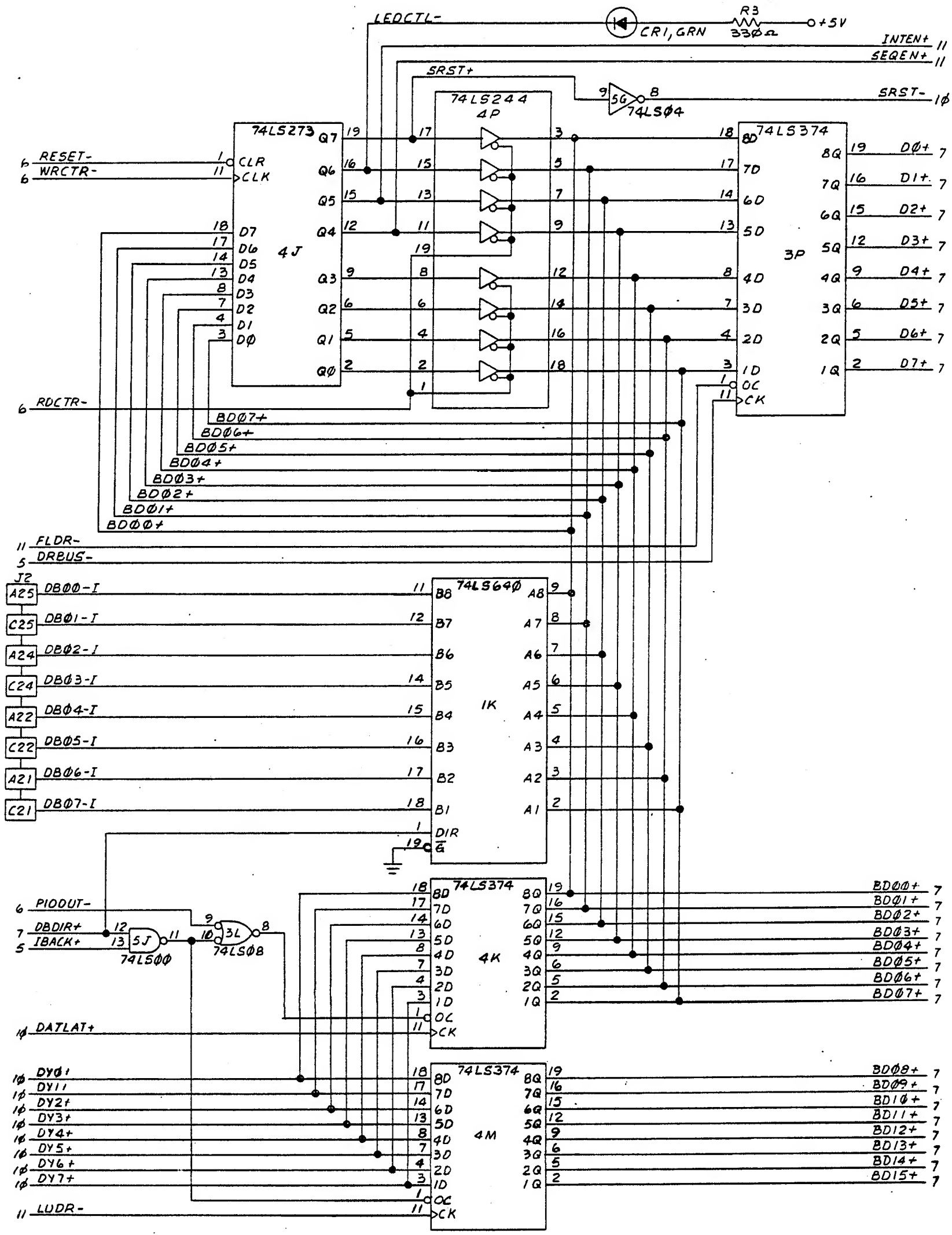


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 9 of 13)

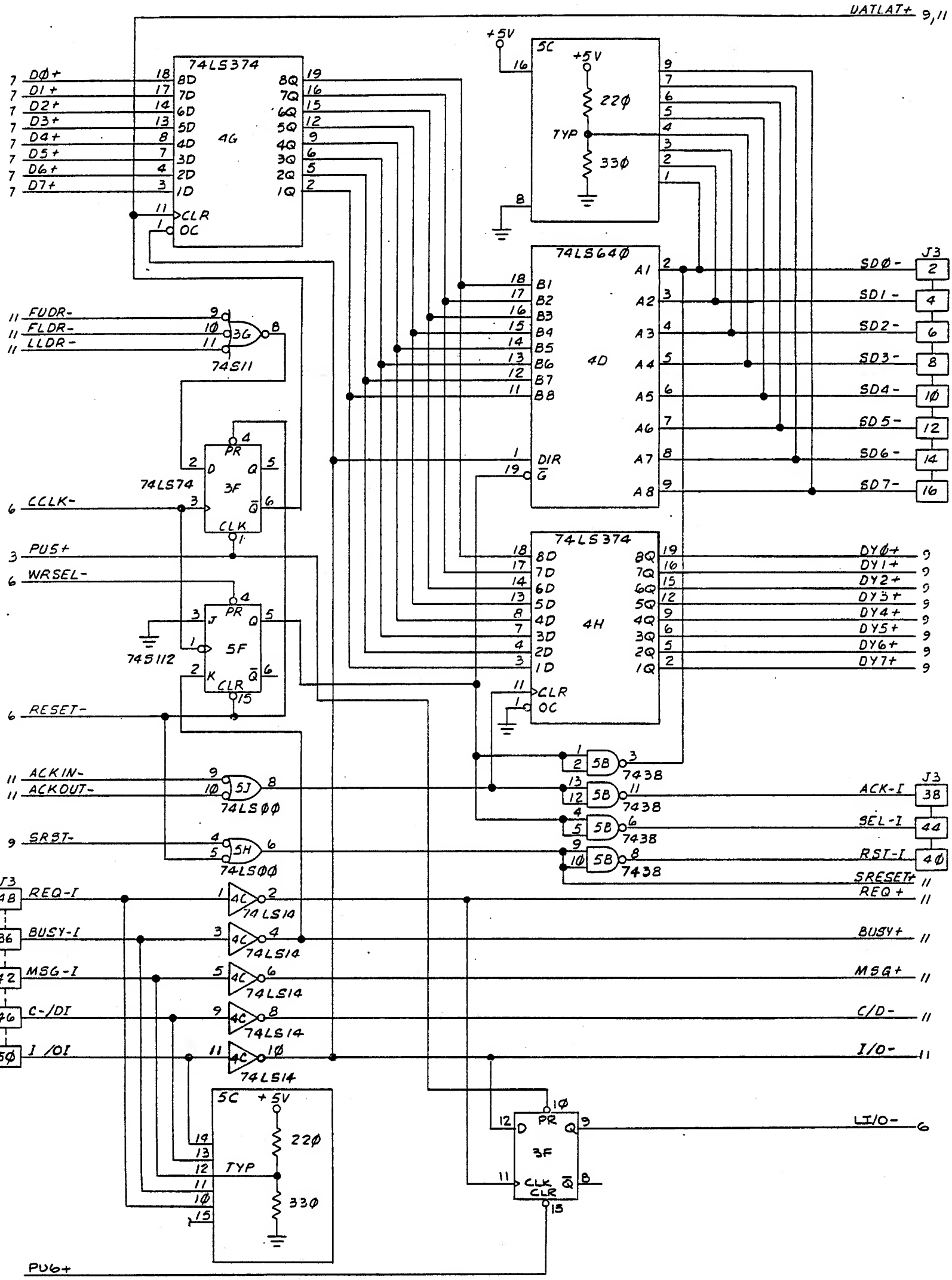


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 10 of 13)

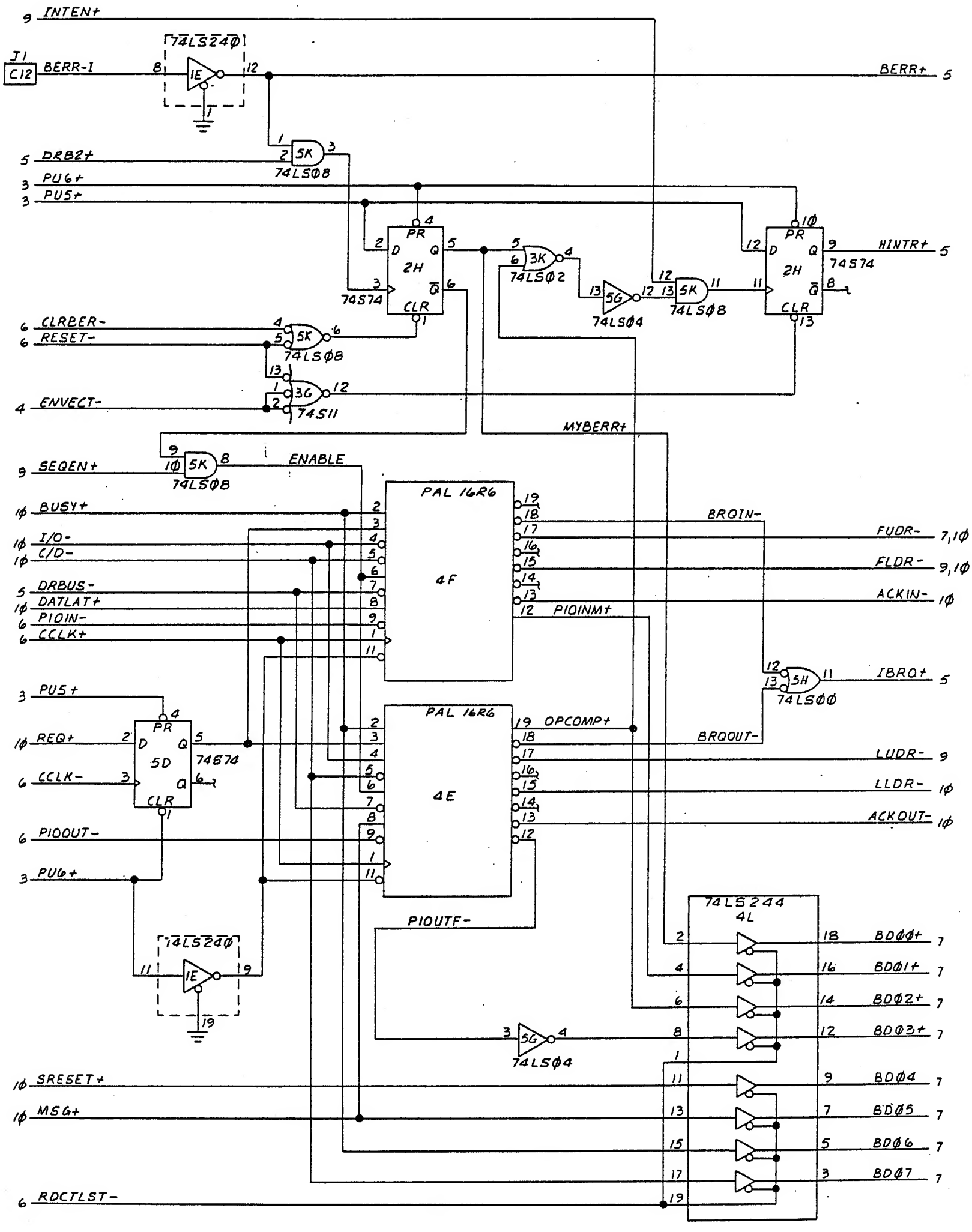


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 11 of 13)

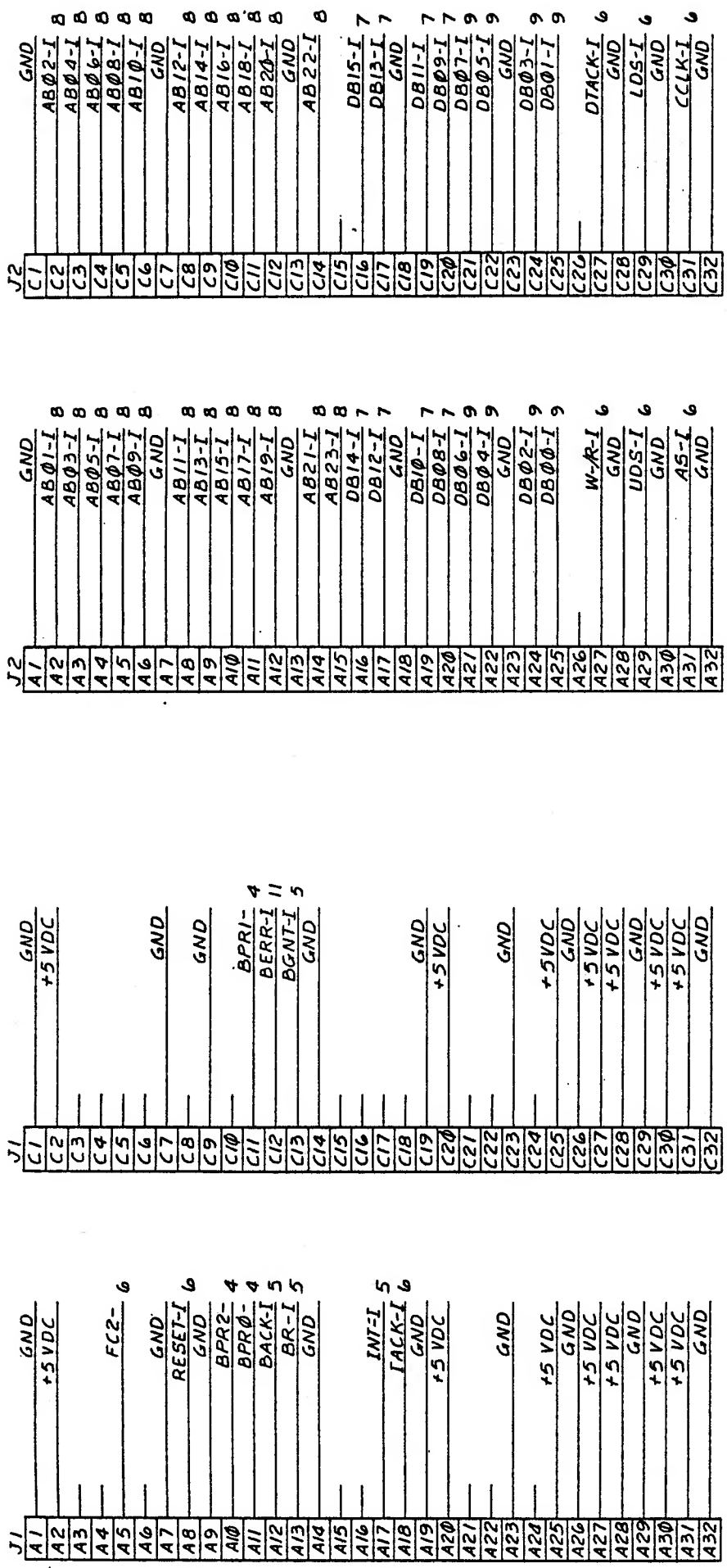


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 12 of 13)

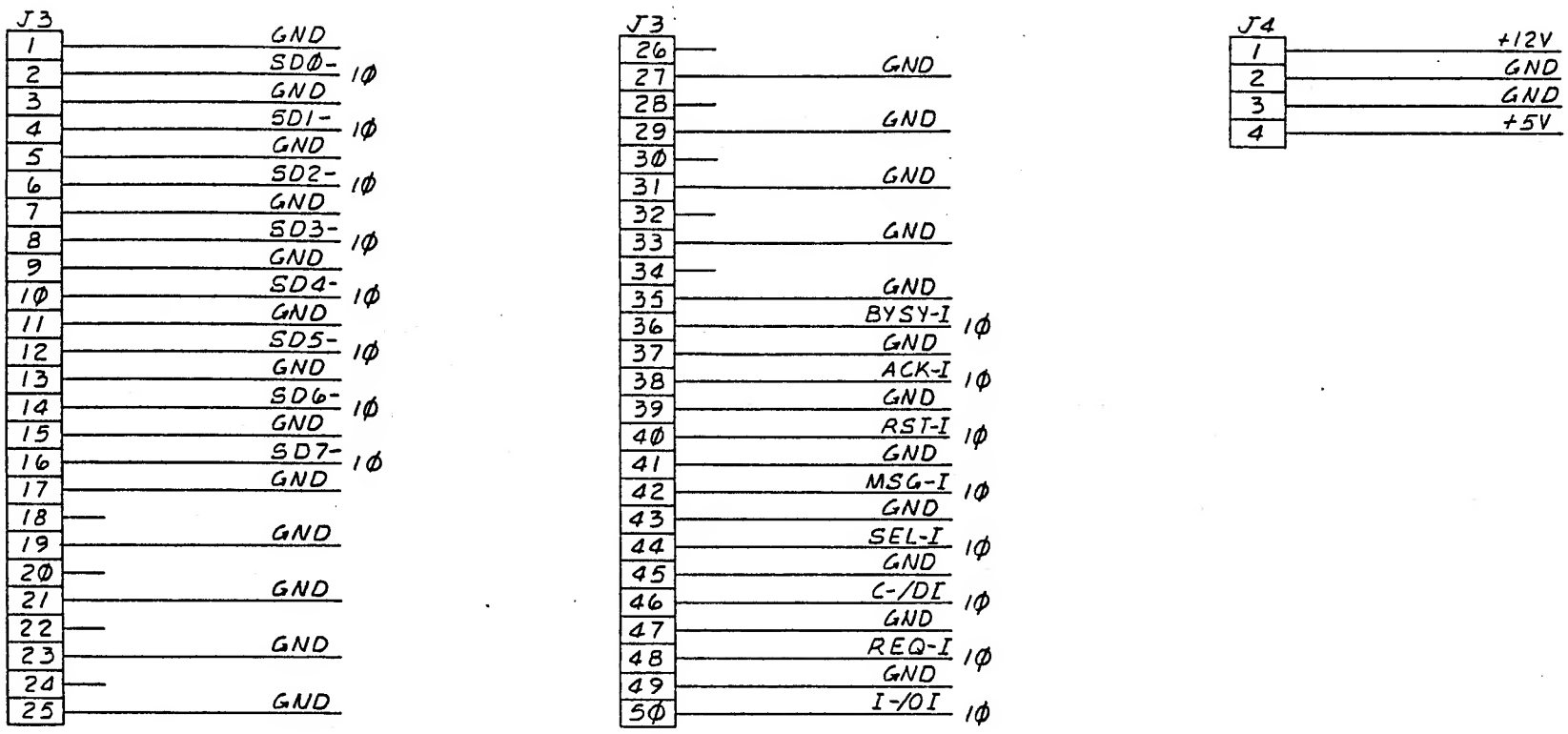


Figure B-10. Part No. 903439-001, Logic Diagram (Sheet 13 of 13)

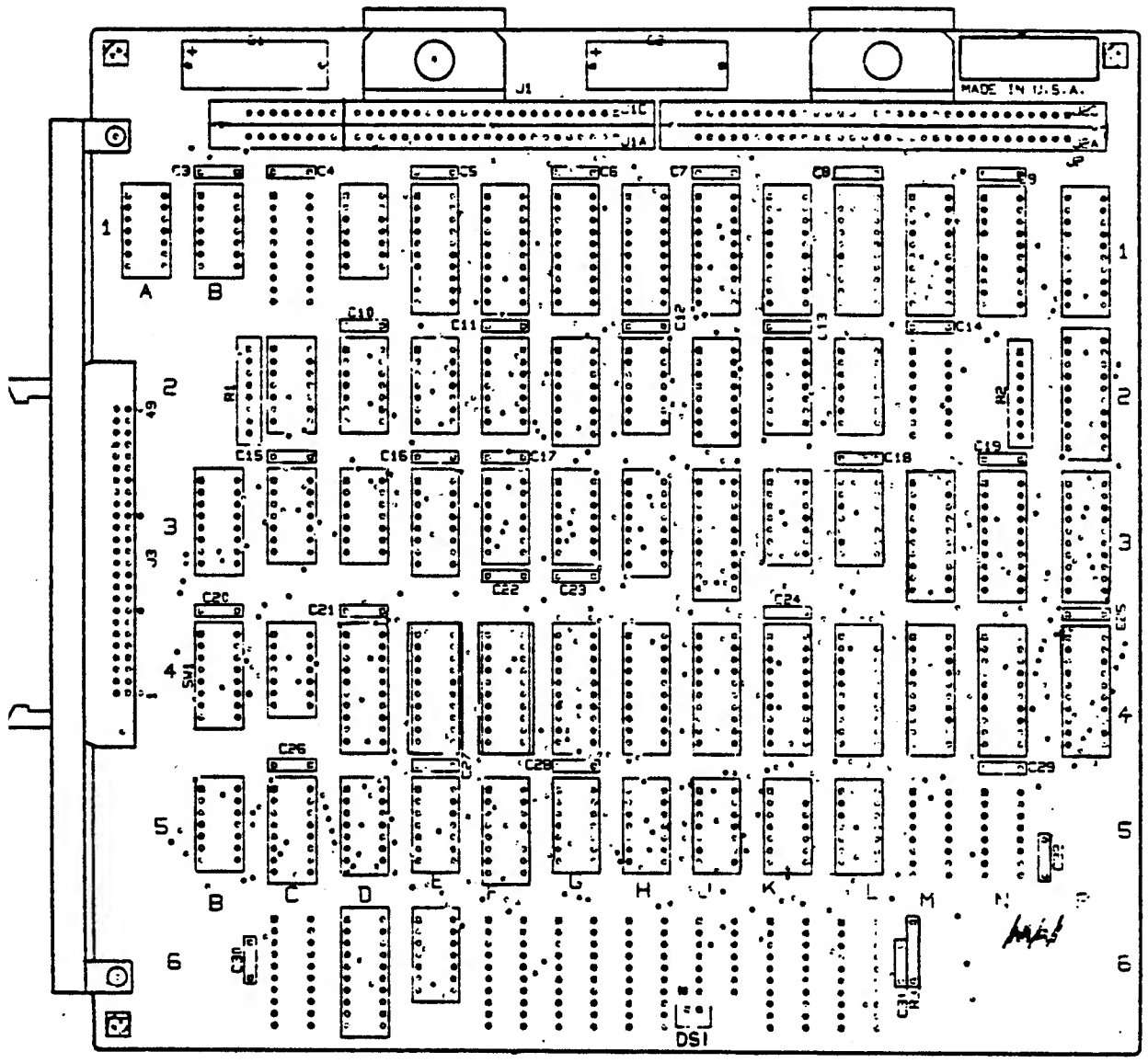


Figure B-11. Part No. 907649-001, Parts Location Diagram

Table B-6. Part No. 907649-001, List of Parts (Sheet 1 of 2)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0001	905150-001	PCB BUS ADAPT 1/2" STREAMER CONTROLLER	*
0003	762022-003	LABEL TAB .375X1.250 YEL	*
0005	101514	IC 7438 BUFFER QUAD 2 INPUT NAND	5B
0007	101709	IC 74LS00 QUAD 2-IN NAND	5H,5J
0008	101710	IC 74LS02 QUAD 2 IN NOR	3K
0009	101711	IC 74LS08 QUAD 2INP AND	3L,5K
0010	101656	IC 74LS04 HEX INVERTER	5G
0011	161015	IC 74LS14 HEX SCHMITT TRIGGER INVERTER	4C
0014	101740	IC 74LS51 DUAL 2-WIDE 2-IN-&/OR-INVERT	1D
0021	101633	IC SN74S157 QUAD 2-1 LINEDATA SLCT/MUX	3B
0022	161068-001	IC 74LS244 OCTAL BUFFER/LINE DRIVER	4L,4P
0024	161064-001	IC 74LS240 BUFF LINE DR 3-ST OCTAL	1E,3J
0026	161023	IC 74LS273 OCTAL D-TYPE FLIP/FLOP	4J
0027	161065-001	IC 74LS374 OCTAL REGISTER D-TYPE F/F	3N,3P,4H,4K, 4M,4N
0029	161111-001	IC 74LS640 OCTAL BUS TRANS INV 3-STATE	1K,1L,4D
0030	161151-001	IC 74LS699 SYNC U/D COUNT/REG	1J,1M,1N,1P, 2P,3M
0033	101315	IC 74S00 QUAD 2 INPUT POS NAND GATE	5L
0034	101655	IC 74S02 POS-NOR GATE TOTEM-POLE	2D,3C
0035	101623	IC 74S11 3 INPUT AND	3G
0036	101625	IC 74S32 QUAD 2 INPUT POSITIVE-OR GATE	2K
0037	101627	IC SN74S38 QUAD 2 INPUT POS NAND BFFR	1A,2F
0038	101615	IC 74S08 QUAD 2 INPUT POS AND GATE	2L
0039	101628	IC 74S64 4-2-3-2 INPUT AND/OR INV GATE	1B
0041	101629	IC SN74S74 DUAL D-TYPE FLIP/FLOP	2C,2H,3D,5D, 3F,6E
0043	101630	IC 74S112 DUAL J-K EDGE TRIG FLIP/FLOP	3E,5F
0044	161076-001	IC 74S133 13 INP NAND	2G
0045	101631	IC 74S138 DECODER/DEMULTIPLEXER	2J,3H
0046	161009	IC 74S240 OCTAL BUFFER 3-STATE TTL	1F,1G,6D
0047	101637	IC SN74S260 DUAL 5 INPUT POS-NOR GATE	2E
0048	161074-001	IC 74S244 OCTAL BUFFER	1H
0050	161006	IC 74S374 OCTAL D-TYPE FLIP/FLOP	4G
0051	101671	IC 74S280 9 BIT ODD/EVEN PARITY GEN	5E
0055	911006-009	IC PAL SCSI TAPE ADAPT CONT/HOST SEQR	4E
0056	911009-004	IC PAL WDC HOST/CONTROLLER SEQUENCER	4F
0061	119001-002	RES NTWK SIP 8 PIN 7 RES 1.0K OHM	R1,2
0062	119009-004	RES NTWK DIP 16 PIN 28 RES 220/330 OHM	5C
0075	104010-001	CAP CERAMIC Z5U AXL .1UF +80 -20% 50V	C3-32
0076	108016-004	CAP ALUM ELECT 100UF +75 -20% 6V	C1,2
0080	300092-001	CONN DIN FML 3X32 PRESS-FIT 64 POS A&C	J1,2
0081	310019-001	CONN HOUSING/GUIDE DIN 3X32 .100CTS ML	(J1,2)
0082	325003-061	CONN HDR .025SQ PCB 50POS RA W/LG LTCH	J3
0084	907388-001	EJECTOR EURO-DIN CONN STACK	(J1,2)
0085	907769-001	LATCH EURO-DIN CONNECTOR STACK	(J1,2)
0086	907985-001	CATCH PCBA STACK CONTROLLER	(J1,2)
0087	214027-001	FASTENER PUSH-ON .312 DIA STUD	(J1,2)
0090	325005-011	SOCKET IC DIP 4-LEAF CONT GOLD 20 POS	(4F,4E)

Table B-6. Part No. 907649-001, List of Parts (Sheet 2 of 2)

REF NO.	PART NO.	DESCRIPTION	REFERENCE
0095	331014-005	SWITCH DIP SLIDE SPST AUTO-INSERT 8SEC	SW1 (4B)
0096	152001-001	DIODE LIGHT EMITTING GREEN DIFF LENS	DS1
0097	111000-029	RES CARBON FILM .25W 5% 330 OHM	R3
0100	907821-001	COVER PLATE 1/2" STREAMER CONTROLLER	(J3)
0101	208000-001	RIVET BLIND .116DX.188L ALUM	*

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R3	
C32	
DS1	

POWER CHART (UNLESS OTHERWISE SPECIFIED)					
DEVICE	+5V/+5VB ⟨4⟩	GND	+12V	-12V	-5V
ALL 20 PIN	20	10			
ALL 16 PIN	16	8			
ALL 14 PIN	14	7			

Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 1 of 15)

COMPONENT MAP

1A	74S38	4	4	4	
1B	74S64	4			
1C	SPARE				
1D	74LS51	5			
1E	74LS24Ø	5	5	5	5
		6	6	11	11
1F	74S24Ø	6	6	6	6
		6	6	6	1Ø
1G	74S24Ø	6	6	6	6
1H	74S244	6	6	6	6
		6	8	8	8
1J	74LS697	8			
1K	74LS64Ø	9			
1L	74LS64Ø	7			
1M	74LS697	8			
1N	74LS697	8			
1P	74LS697	8			
2C	74S74	4	4		
2D	74SØ2	4	5	5	5
2E	74S26Ø	5	5		
2F	74S38	5	5	5	6
2G	74S133	6			
2H	74S74	11	11		
2J	74S138	6			
2K	74S32	6	6	7	7
2L	74SØ8	7	8	8	8
2P	74LS697	8			
3B	74S157	4			
3C	74SØ2	4			
3D	74S74	5	5		
3E	74S112	5	5		
3F	74S74	1Ø	1Ø		
3G	74S11	4	1Ø	11	
3H	74LS138	6			
3J	74LS24Ø	6	6	6	6
		6	6	6	6
3K	74LSØ2	7	11		
3L	74LSØ8	6	7	9	1Ø
3M	74LS699	8			

3N	74LS374	7			
3P	74LS374	9			
4B	SWITCH	4			
4C	74LS14	1Ø	1Ø	1Ø	1Ø
		1Ø			
4D	74LS64Ø	1Ø			
4E	PAL	11			
4F	PAL	11			
4G	74S374	1Ø			
4H	74LS374	1Ø			
4J	74LS273	9			
4K	74LS374	9			
4L	74LS244	11	11	11	11
		11	11	11	11
4M	74LS374	9			
4N	74LS374	7			
4P	74LS244	9	9	9	9
		9	9	9	9
5B	7438	1Ø	1Ø	1Ø	1Ø
5C	RES NTWK	1Ø			
5D	74S74	11			
5E	74S28Ø	1Ø			
5F	74S112	4	1Ø		
5G	74LSØ4	7	9	11	11
5H	74LSØØ	6	1Ø	11	
5J	74LSØØ	6	9	1Ø	
5K	74LSØ8	11	11	11	11
5L	74SØØ	5	1Ø	12	
5M	SPARE				
5N	SPARE				
6C	SPARE				
6D	74S24Ø	1Ø	12		

6E	74S74	12	12		
6F	SPARE				
6G	SPARE				
6H	SPARE				
6J	SPARE				
6K	SPARE				
6L	SPARE				

Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 2 of 15)

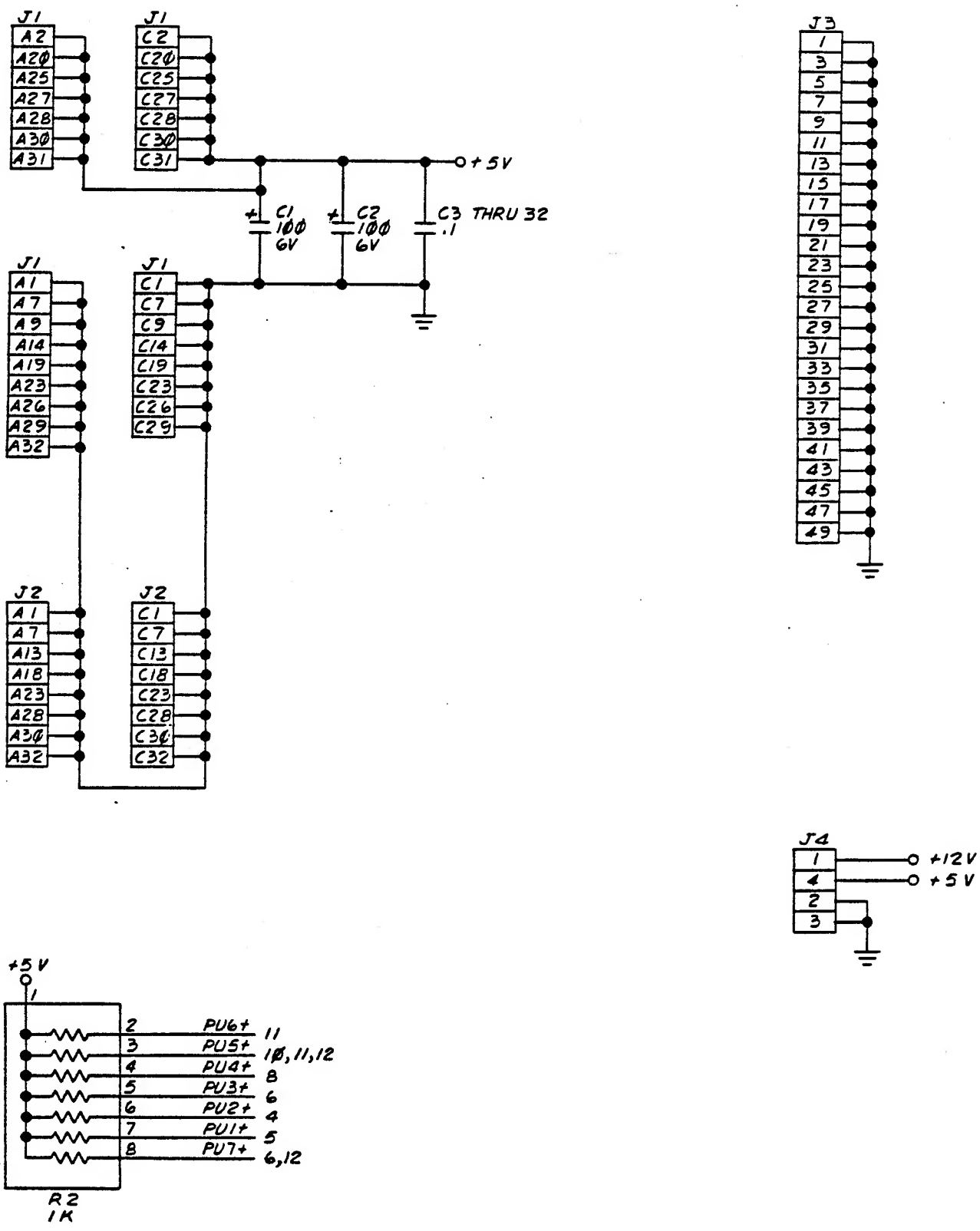


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 3 of 15)

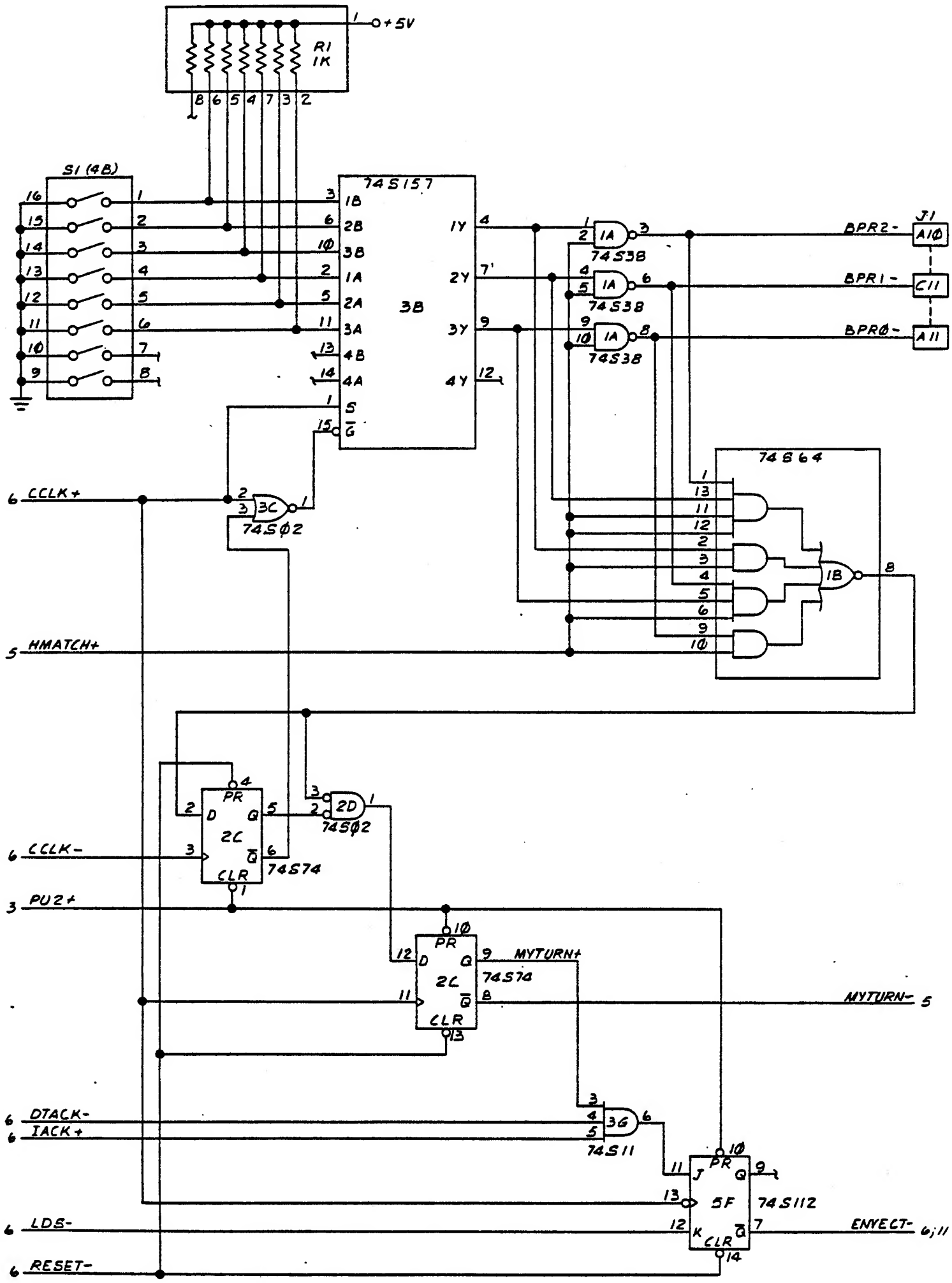


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 4 of 15)

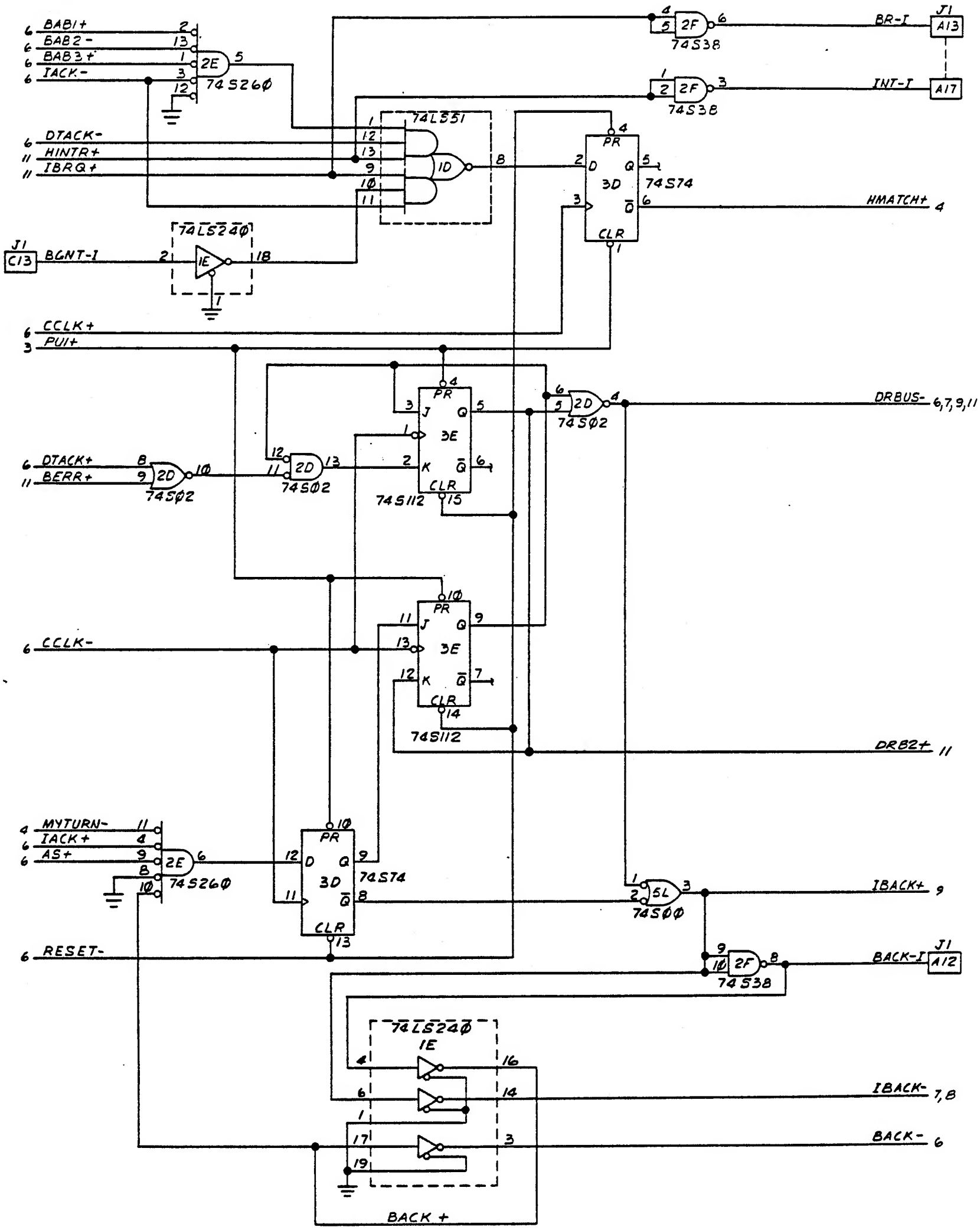


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 5 of 15)

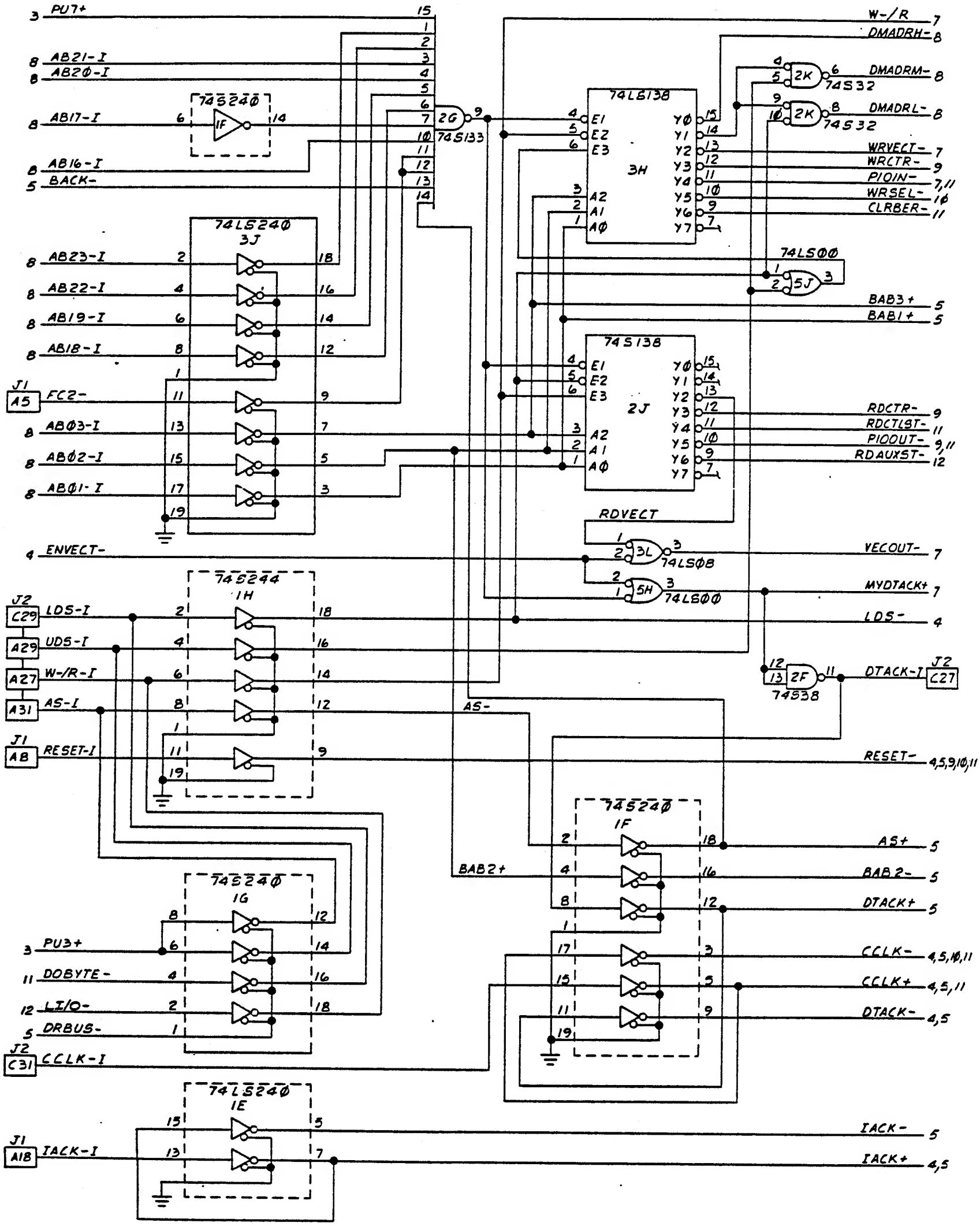


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 6 of 15)

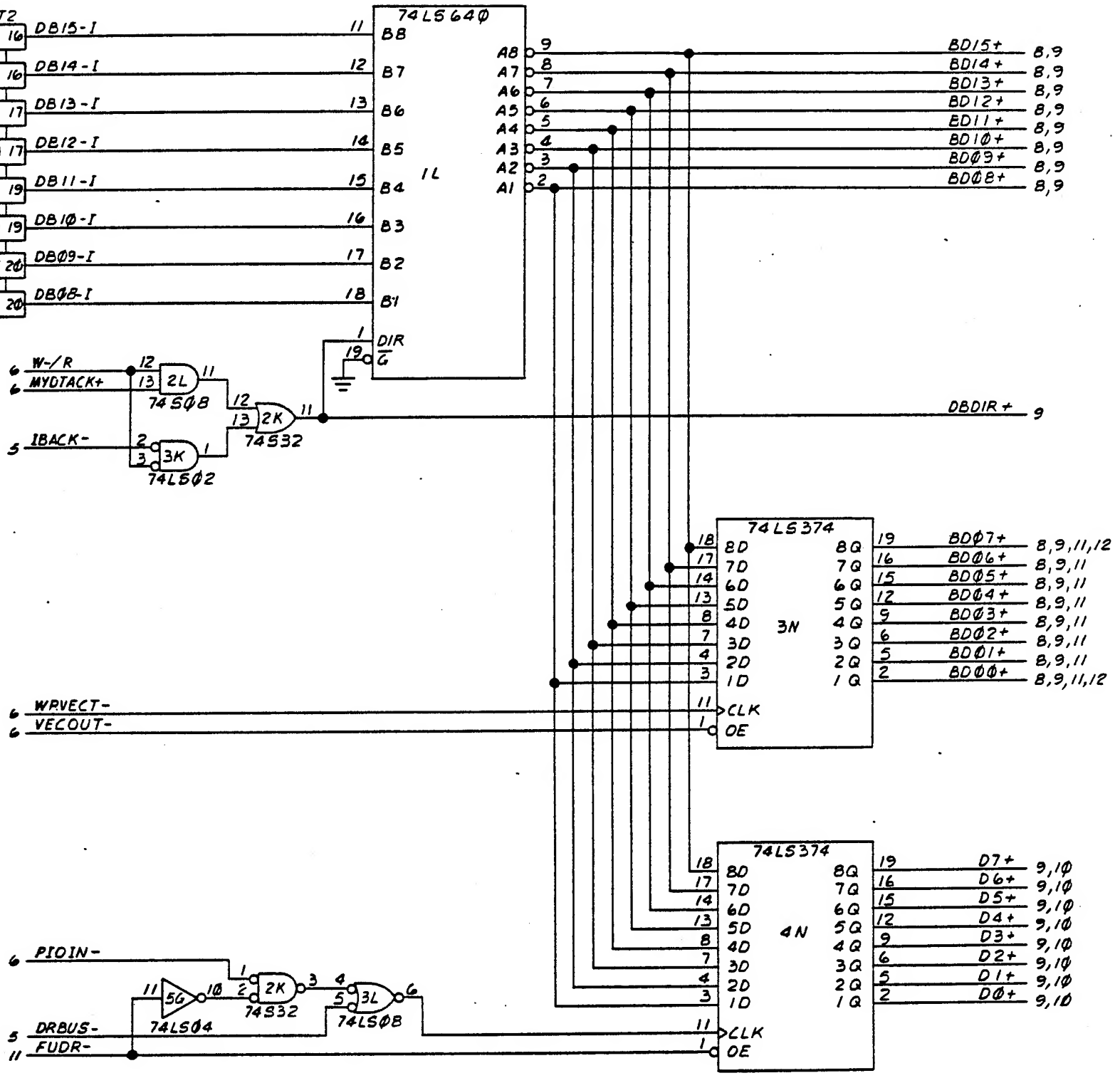


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 7 of 15)

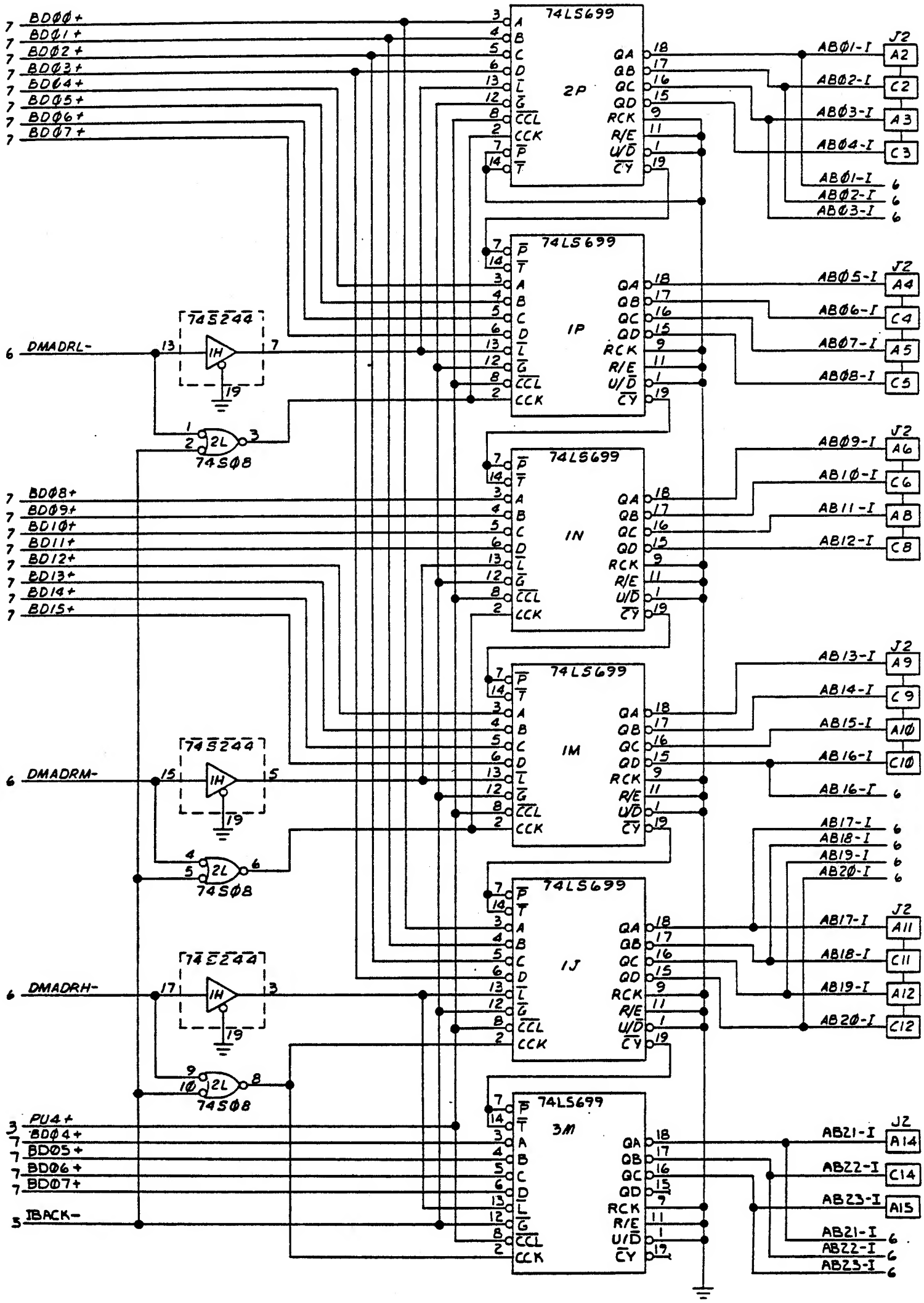


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 8 of 15)

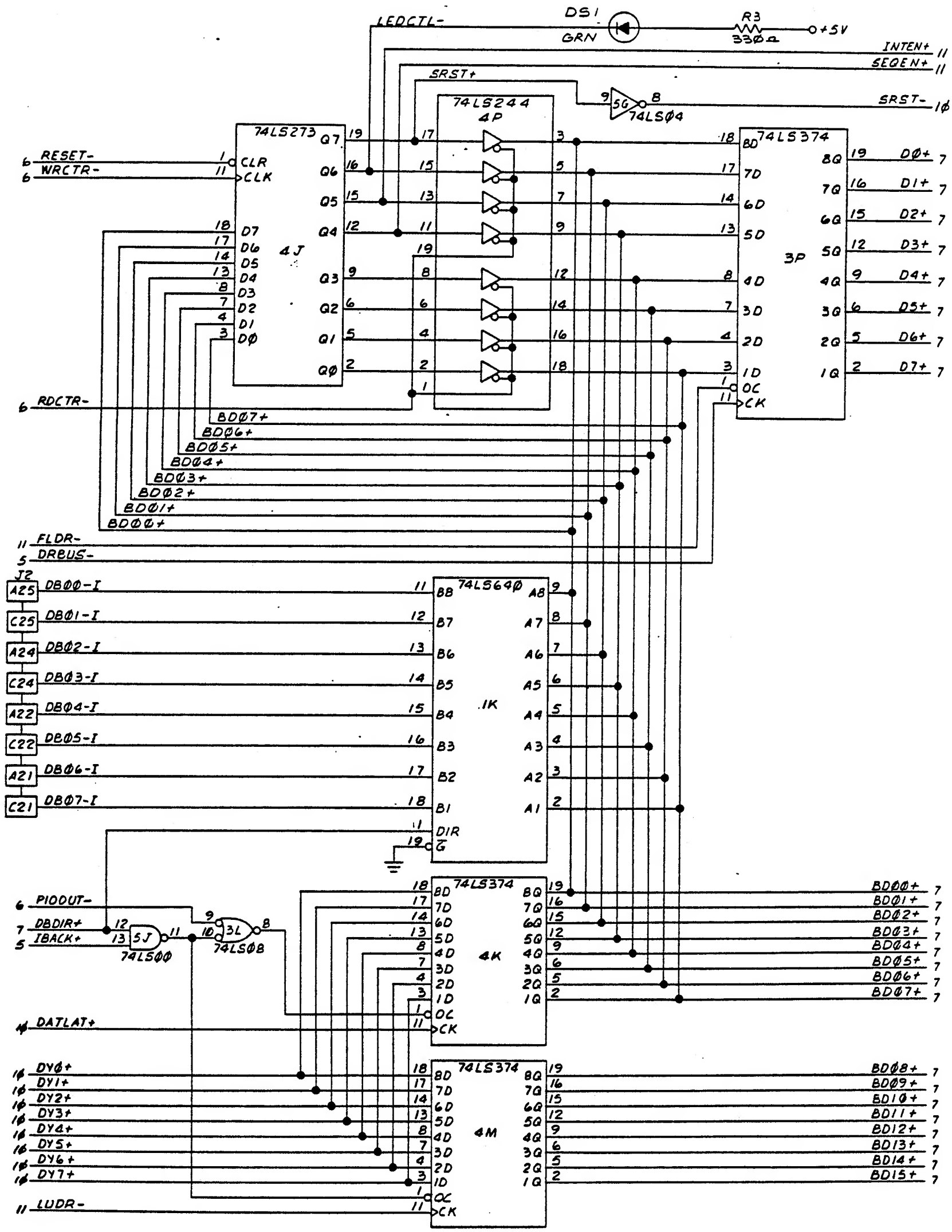


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 9 of 15)

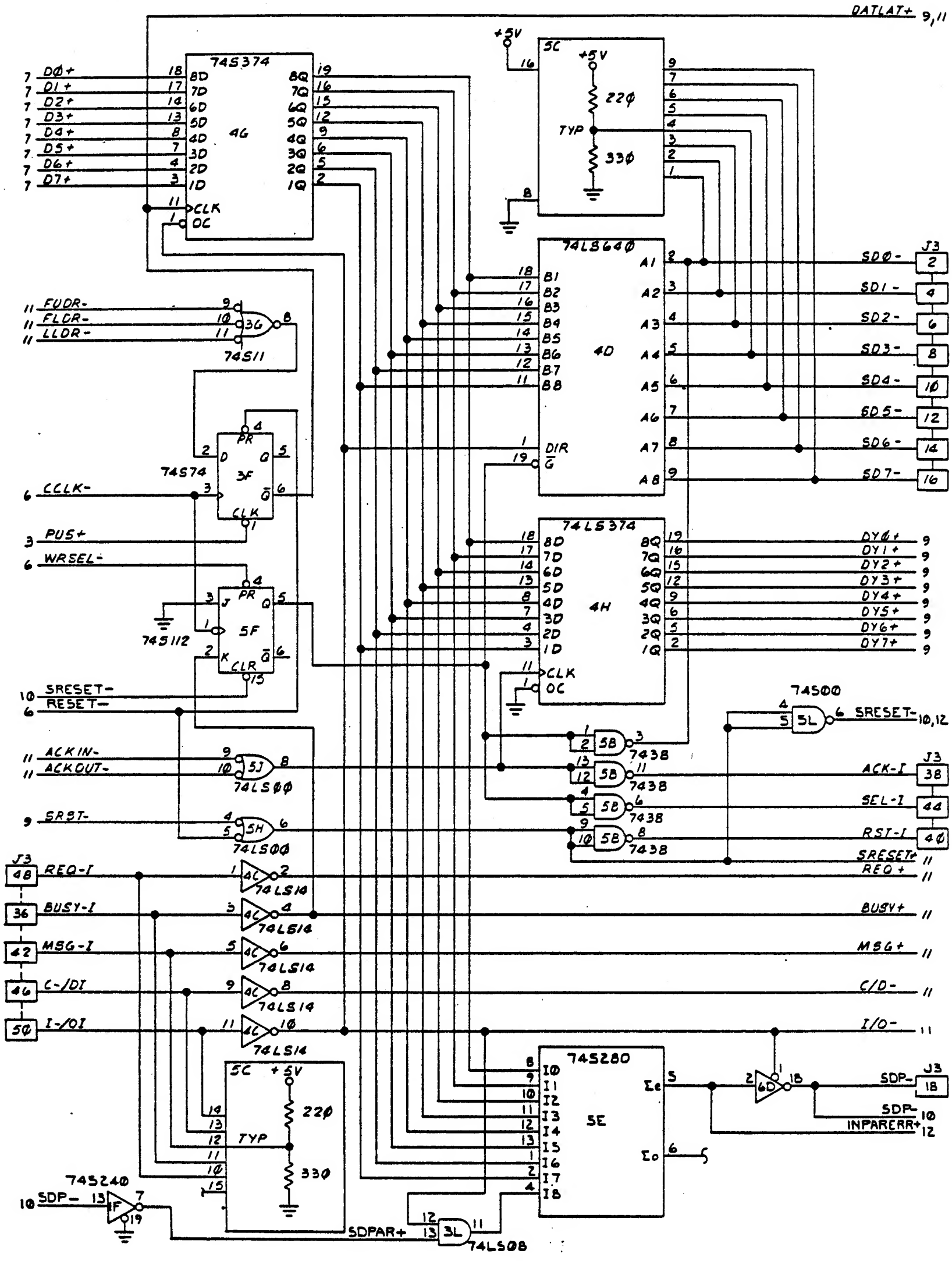


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 10 of 15)

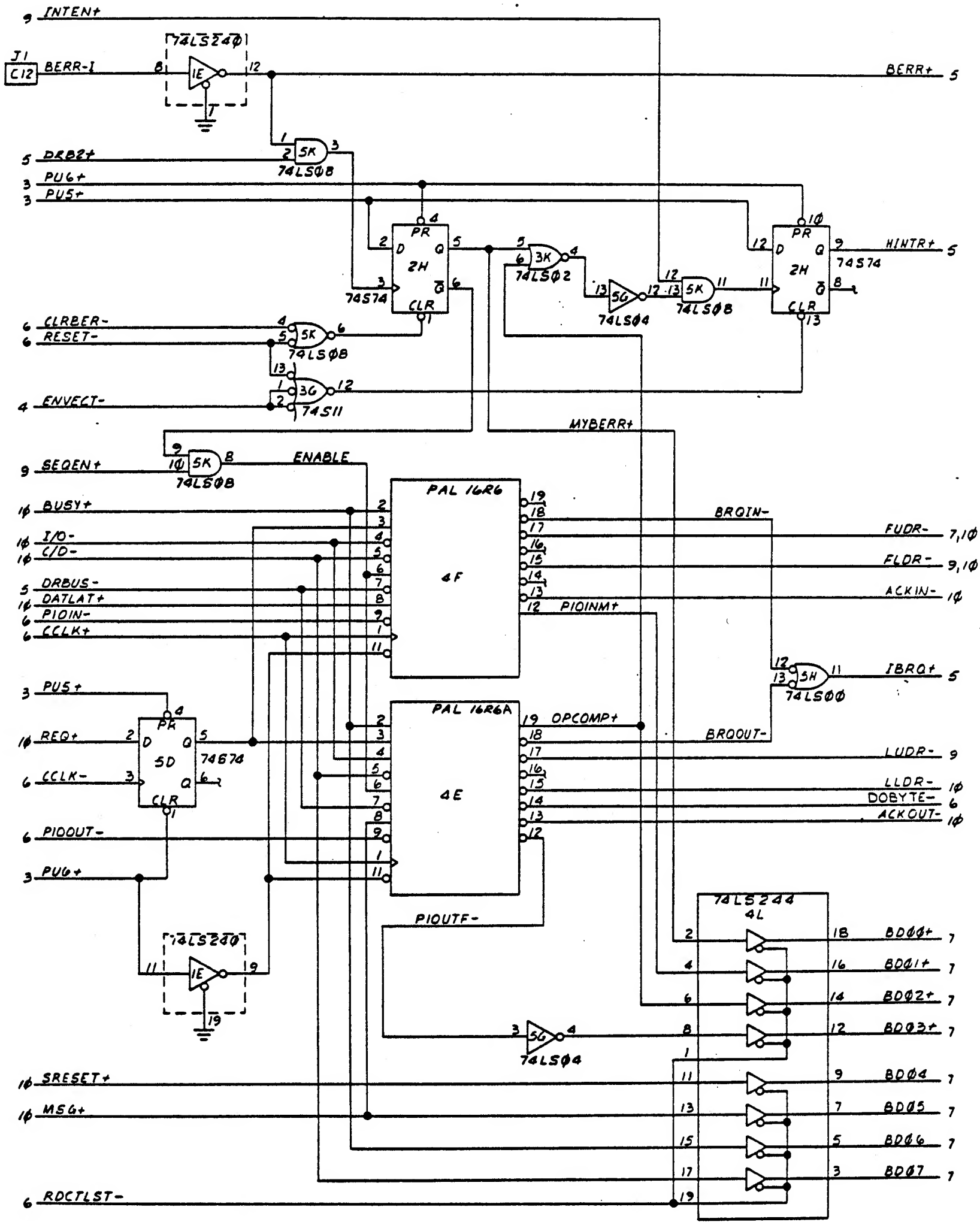


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 11 of 15)

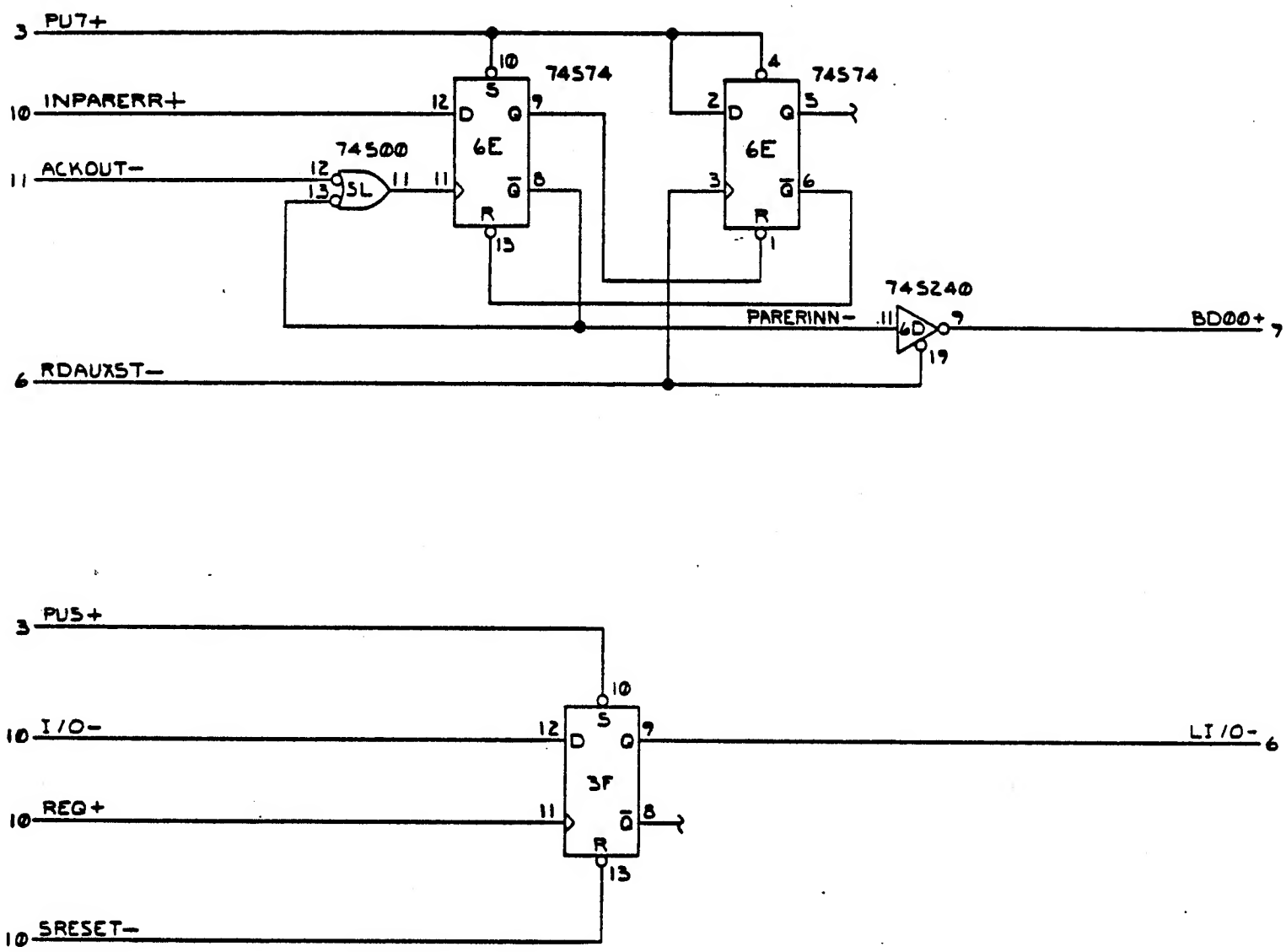


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 12 of 15)

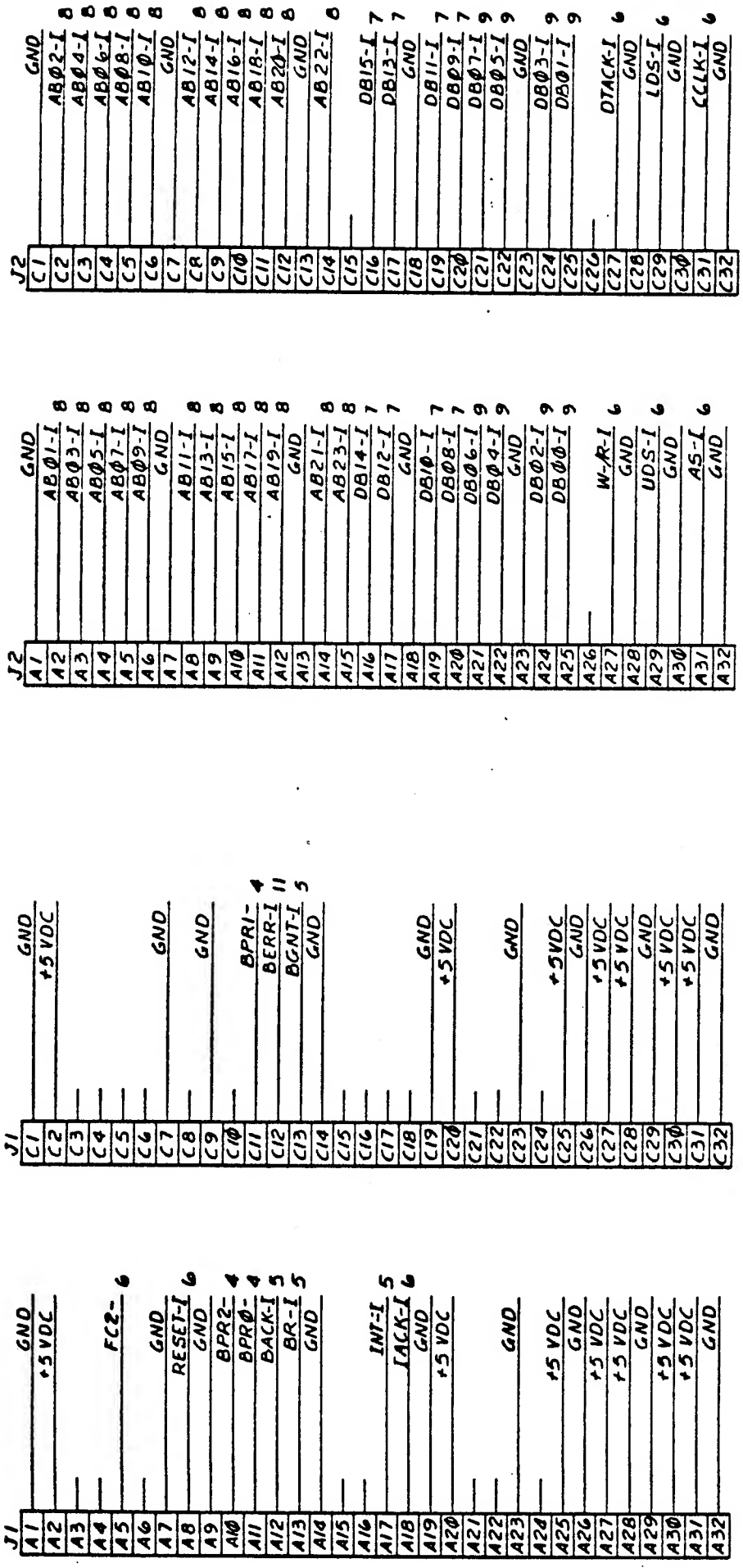


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 13 of 15)

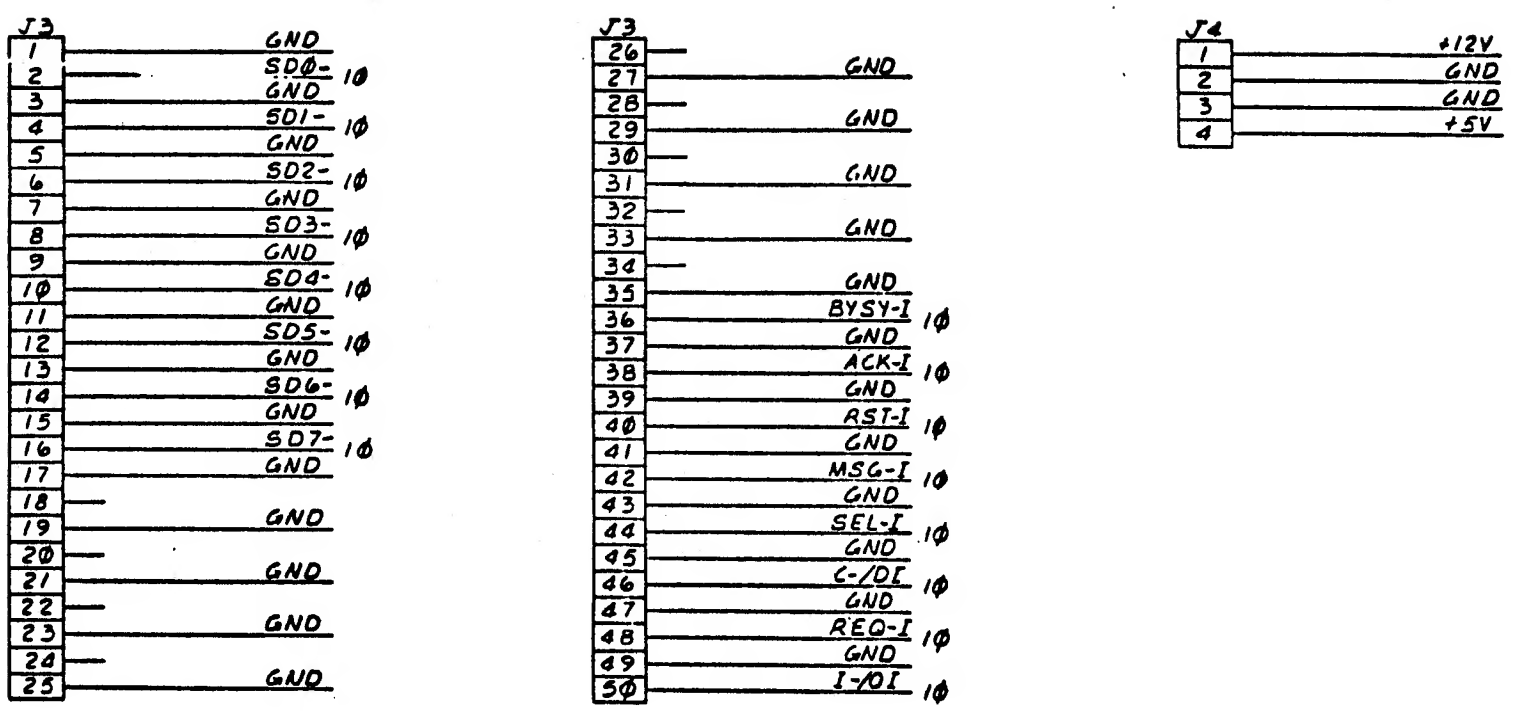


Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 14 of 15)

```
PAL16R6
MASTER PAL WDC HOST/CONT
BFISD PART NUMBER 652036 (RAW PART NUMBER 911008 006)
LOCATION 4F
CCLK    BUSY    REQ     /OUT    /DAT    ENABLE  /DRBUS  DATLAT  /PIOIN  GND
/ENB    /PIOINM /ACKIN  /LDRE   /FLDR   /UDRE   /FUDR   /BRGIN  /PREFET VCC

PREFET  = /ENABLE
        + PREFET * /BRGIN
        + /BUSY

FUDR    := REQ*/UDRE*/LDRE*/PREFET*/DRBUS*/ACKIN*/BRGIN*ENABLE*OUT*DAT
         + REQ  *  PIOIN
         + FUDR *  /ACKIN * ENABLE
         + PIOIN * /BUSY * /ENABLE * /LDRE  * /FLDR
         + LDRE  * /BUSY * /ENABLE * /DRBUS * /UDRE

UDRE    := FUDR *  ENABLE * OUT * DAT * /PIOIN * REQ
         + UDRE *  ENABLE * /DRBUS * BUSY
         + FUDR * /ENABLE * /BUSY * LDRE
         + UDRE * /ENABLE * /BUSY * /FLDR

FLDR    := REQ  *  ENABLE * OUT * DAT * UDRE * /LDRE * /ACKIN
         + FLDR *  ENABLE * BUSY * /ACKIN
         + PIOIN * /BUSY * /ENABLE * LDRE

LDRE    := FLDR *  ENABLE * OUT * DAT * REQ
         + LDRE *  ENABLE * /DRBUS * BUSY
         + DRBUS * /BUSY * ENABLE
         + LDRE  * /FLDR * /BUSY

ACKIN   := REQ  *  DATLAT
         + REQ  *  ACKIN
         + DATLAT * /BUSY

BRGIN   := REQ  *  PREFET * ENABLE * OUT * DAT
         + REQ  *  UDRE   * /LDRE  * OUT * DAT * /ACKIN * ENABLE
         + BRGIN * /DRBUS * ENABLE
         + PIOIN * ENABLE * /BUSY * PREFET

PIOINM  = /REQ
        + /OUT
        + ACKIN
```

```
PAL16R6
MASTER PAL SCSI TAPE CONT/HOST
BFISD PART NUMBER 652094 (RAW PART NUMBER 911006-009)
LOCATION 4E  (CHECKSUM = 6ADC)
CCLK    BUSY    REQ     OUT     /DAT    ENABLE  /DRBUS  MSG     /PIOOUT GND
/ENB    /PIOUTF /ACKOUT /DOBYTE /LLDR   /UDRF   /LUDR   /BRGOUT /OPCOMP VCC

PIOUTF  = ACKOUT  * ENABLE  * /PIOOUT * BUSY    * /LUDR * /LLDR * DAT
        + /ACKOUT * /PIOOUT * REQ     * /DAT    * OUT
        + /ENABLE * /PIOOUT * REQ     * DAT     * OUT   * /ACKOUT
        + PIOUTF  * /LLDR   * /LUDR   * BUSY

LUDR    := PIOUTF  * /UDRF  * ENABLE * /BRGOUT * /DRBUS * OPCOMP * BUSY * DAT
         + LUDR    * PIOUTF * ENABLE * BUSY
         + LUDR    * ACKOUT * BUSY   * ENABLE  * DAT

UDRF    := LUDR    * ENABLE * BUSY   * DAT
         + UDRF    * ENABLE * BUSY   * /DRBUS

LLDR    := PIOUTF  * UDRF   * ENABLE * /BRGOUT * BUSY * /LUDR * DAT
         + LLDR    * PIOUTF * ENABLE * BUSY
         + PIOUTF  * PIOOUT
         + PIOOUT  * /BUSY  * /ENABLE
         + LLDR    * ACKOUT * BUSY   * ENABLE  * DAT

ACKOUT  := REQ     * /PIOUTF * OUT * ENABLE * DAT * /LUDR * /LLDR
         + REQ     * PIOOUT  * OUT * PIOUTF
         + ACKOUT  * REQ
         + /BUSY   * PIOOUT

BRGOUT  := UDRF    * LLDR    * ENABLE  * BUSY * DAT * /DRBUS
         + BRGOUT  * /DRBUS  * ENABLE  * BUSY
         + UDRF    * OUT     * /DAT    * /MSG * REQ * /DRBUS

OPCOMP  = /REQ
        + /OUT
        + DAT
        + BRGOUT
        + UDRF

DOBYTE  := UDRF   * OUT  * /DAT * /MSG * REQ * BUSY
         + DOBYTE * /MSG * BUSY
```

Figure B-12. Part No. 907649-001, Logic Diagram (Sheet 15 of 15)

NOTES